ASMII Production readiness review (PRR) document
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Abstract:
CSC electronic specifications are discussed. ASMII design evolution and final design with schematic is presented. Layout strategies, COTS and ASIC qualification status and plans, production plan, ASMII test procedures, test system, quality assurance, quality control and burn in plan are presented.

ASMII Introduction:
All on chamber signal processing for Atlas CSCs, excluding preamplification and shaping is performed on ASMII. ASMII is a 10-layer, double sided printed circuit board, with components on top and bottom layers, serving total of 192 CSC channels, 96 channels each from two different CSC layers. Main components on ASMII include 3 different custom ASICs and 7 different COTs which include the ST positive voltage regulators. There are four precision ASMIIs and one transverse ASMII per chamber. Signals from the preamp/shaper are sent to the ASMII from the ASMI through a surface mount connector. Each preamp transmits 24 channels to 2 SCAs. The Atlas LAr Calorimeter SCA is used in muon mode, where cells are continuously read-out to a dedicated ADC. The SCA outputs are then quantized to 12-bits by Analog Devices AD9042 ADCs. It has 16 hamac muon SCAs (Switched Capacitor Arrays/Analog Memory), equal number of 12 bit ADCs converting signals at 6.66MHz from corresponding SCA. The complete signal chain on ASMII can be summarized as 12 channels of each of the 16 SCAs are time multiplexed and then digitized using a 12bit ADCs, at 6.66MHz. Custom ASIC, ASM2MUX converts 24bits coming in at 6.66MHz from two adjacent ADCs from the same layer of the board, into 4 bits out at 40MHz. Such four 4 ASM2MUXs multiplex data from 4 pairs from the same board layer to one serializer link, where a pair of ADCs then occupies four data lines each of one G-Link serializer. The G-Link serializers are configured to operate with a 16-bit input word in the single frame mode at a frame rate of 40MHz. There are two serializer G-Links, each supporting data transmission of 4 ASM2MUXs. An optical receiver link is used to receive control signals and clocks for the SCAs, ADCs and ASM2MUXs. Control and clocks for SCAs are distributed through MC10H116 PECL buffers, differentially. ADCs are also clocked differentially to minimize noise induced due to single ended clock with a full TTL swing. Custom clock fanout ASIC is used to distribute 40MHz and 6.66MHz clocks to ASM2MUXs and 40MHz clocks to two G-Link serializers. Seven LHC-7913 adjustable positive voltage regulators distribute +5V, +3.3V and +4.1V.

CSC Electronics Specifications:[1]

Noise performance requirements:
Muons generate about 75 electron-ion pairs (Landau peak). About 12% of charge is collected by the precision cathode in 100ns. The average signal size expected is 144fC where the central strip of the cluster receives approximately half of the charge or 72fC. The electronics noise should not degrade the position resolution of the system. The required input referred noise as a function of the average charge is calculated by the following expression:

$$\sigma_{X,\,elec} = \frac{\sqrt{3}.d.ENC}{Q_\lambda} \leq 33\mu m \qquad (1)$$

Where d = strip pitch, ENC = equivalent input noise charge, and Q_λ = total charge induced on cathode plane. From this expression the calculated required noise limit is:

$$ENC \leq 0.5\,fC = 3100e \leftarrow \text{Total input referred noise} \quad (2)$$

The required signal to noise ratio is calculated as:

$$SNR\max strip = \frac{Q_{\lambda,\,cent}}{ENC} = \frac{72\,fC}{3100e} = 145 \quad (3)$$

The dynamic range required for 98.5% efficiency is calculated as follows:

$$\frac{Q_{fs}}{Q_m} \geq 5, \therefore Q_{fs} \geq 5.Q_m = 725.ENC \approx 360\,fC \quad (4)$$

Where, Q_{fs} is the full scale charge. Preamp/shaper gain for V_{FS} (positive lobe of bipolar waveform) is defined as:

$$\Pr eamp/Shaper\ gain = \frac{V_{FS}}{Q_{FS}} = 4.7mV/fC \quad (5)$$

Quantization noise as a function of the full-scale charge and total input referred noise can be calculated by:

$$\frac{Q_{FS}}{2^\wedge Nbits.\sqrt{12}} << ENC \therefore Nbits >> 7.7 \quad (6)$$

High rate performance:
The L1 trigger incurs a latency that includes cable delay and electronics processing by the TIM module and the off-chamber back of crate cards. This latency is estimated to be 98 bunch crossings. Additional latency is incurred by signal propagation from off-chamber to on-chamber electronics and the readout latency of the SCA. An additional 27 bunch crossings is estimated for this latency. The total estimated latency is 125 bunch crossings. The worst-case latency condition occurs for the maximum L1 trigger burst rate defined as eight consecutive triggers each paced at 125ns intervals. The SCA is read-out at a rate of 6.67 MHz (150ns). Since 15 clock cycles are required to readout one time sample the 8th trigger arrives before the first time sample of the first trigger is readout. Beam studies have indicated that four time samples are adequate [1]. Pipeline depth required for eight triggers would then be 32 bunch crossings. The pipeline depth of the SCA is 144 bunch crossings. Since the L1 trigger latency has been estimated as 125 bunch crossings and the required pipeline for an eight trigger burst is 32 bunch crossings the SCA pipeline depth of 144 bunch crossings is not adequate. To circumvent this problem we have chosen to sample at a rate of one-half the bunch crossing rate or 20 MHz. The SCA pipeline depth is effectively doubled to 288 bunch crossings. ASMII support both 20MHz and 40MHz sampling, in such, that 20MHz sampling mode, same SCA location will be clocked twice, and more recent of the two samples will be retained.

Design evolution:
ASMII board has undergone three iterations. The first design version of Amplifier Shaper Module II-ASM II a was completed by January of 2001 at the instrumentation division. The purpose of this version was to develop an ASM board quickly that will serve as a

test-bed for the CSC front end electronics and SCA controller development. This included the characterization of the NEVIS SCA, AD9042 ADC and Pre-Amp. This was a 24 channel board. Second version, ASMII-B was designed to use the SCA Controller developed for the version 'A' and implement it for 192-channels, to establish and test the interface between the preamps and the SCAs, characterize noise, test the G-Links and define its operating mode and establish the readout architecture. This board had an on board SCA controller implemented in an Altera Apex FPGA. Third and final iteration of the board is ASMII-C.

ASMII-C Design:
      Figure: 1

Analog Signal flow on ASMII
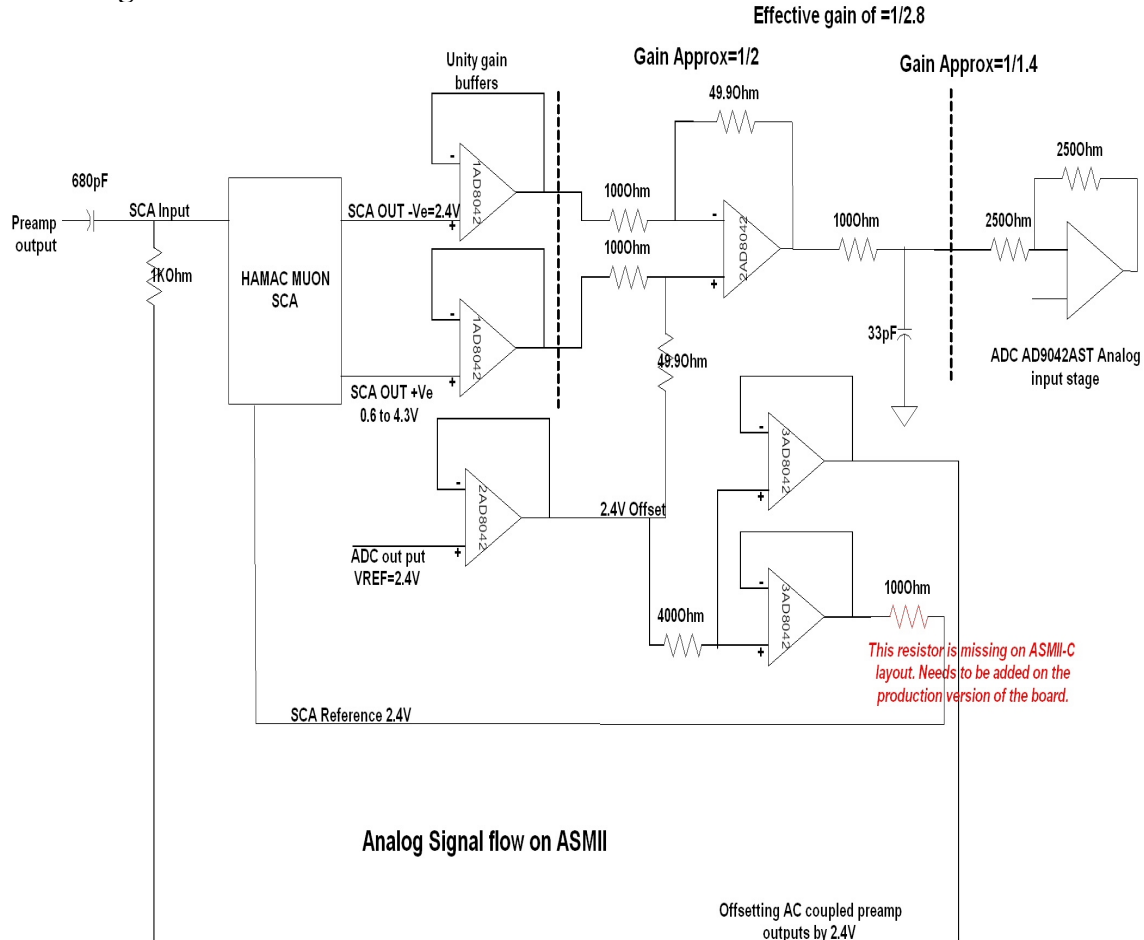
Preamp output pulse positive lobe peaks at 3.25V approximately from a 1.9V baseline, and negative lobe valleys at 0.6V approx. SCAs when used in Muon mode have input dynamic range of 0.4V to 4.3V. In order to utilize maximum of this range, preamp outputs are AC Coupled and are offset to 2.4V. SCAm reference pipeline, is biased at 2.4V. SCAp and SCAm outputs are buffered using AD8042. These two buffered signals are then subtracted and divided by a gain of 1 /2.8 to make the signal fall within the 1V pp input range of ADC. This gain of 1 /2.8 is divided in two stages. Differential stage gain is tuned at 1/ 2. ADC has input impedance of 250Ohm. A series resistor of 100Ohm between ADC and the input impedance of 250Ohm gives a gain of 1/1.408. This resistance is tuned to minimize the noise and to get the right gain.

Following 2.4V offset voltages are derived from the VREF output of AD9042AST. SCA reference pipeline is biased at 2.4V. AC Coupled preamp outputs are offset to 2.4V. +Ve input to the difference amplifier with a overall gain of 1/2.8 is offset at 2.4V to bring the signal level to the dynamic input range of the ADC of 1V centered at 2.4V.

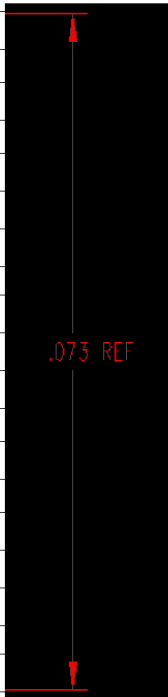Routing of preamp outputs:

ASMII Layer map.
Dimensions are in inches

.0007	TOP: Preamp Signals, Analog signals
.0047	
.0013	L2: AGND
.0080	
.0013	L3: Digital routing
.0080	
.0013	L4: AGND,DVCC
.0060	
.0013	L5: 3.3VD, 5VA, 5VA2
.0080	
.0013	L6: 5VA1, 5VD, 5VD1
.0060	
.0013	L7: GND, 5VD1
.0080	
.0013	L8:SCA control signals, 5VA2
.0080	
.0013	L9:GND
.0047	
.0007	BOTTOM: Preamp Signals, Analog signals

.073 REF

Figure:2

Preamp outputs and all the sensitive analog signals are routed on the top and bottom layers of the board which are isolated from the inner layers with solid ground planes on layers 2 and 9. SCA control signals are routed on layer 8. Rests of the layers are split and allocated areas for 7 different power planes is proportional to the currents carried by them. Routing is done with an utmost care to isolate noise sensitive analog signals from digital activity.
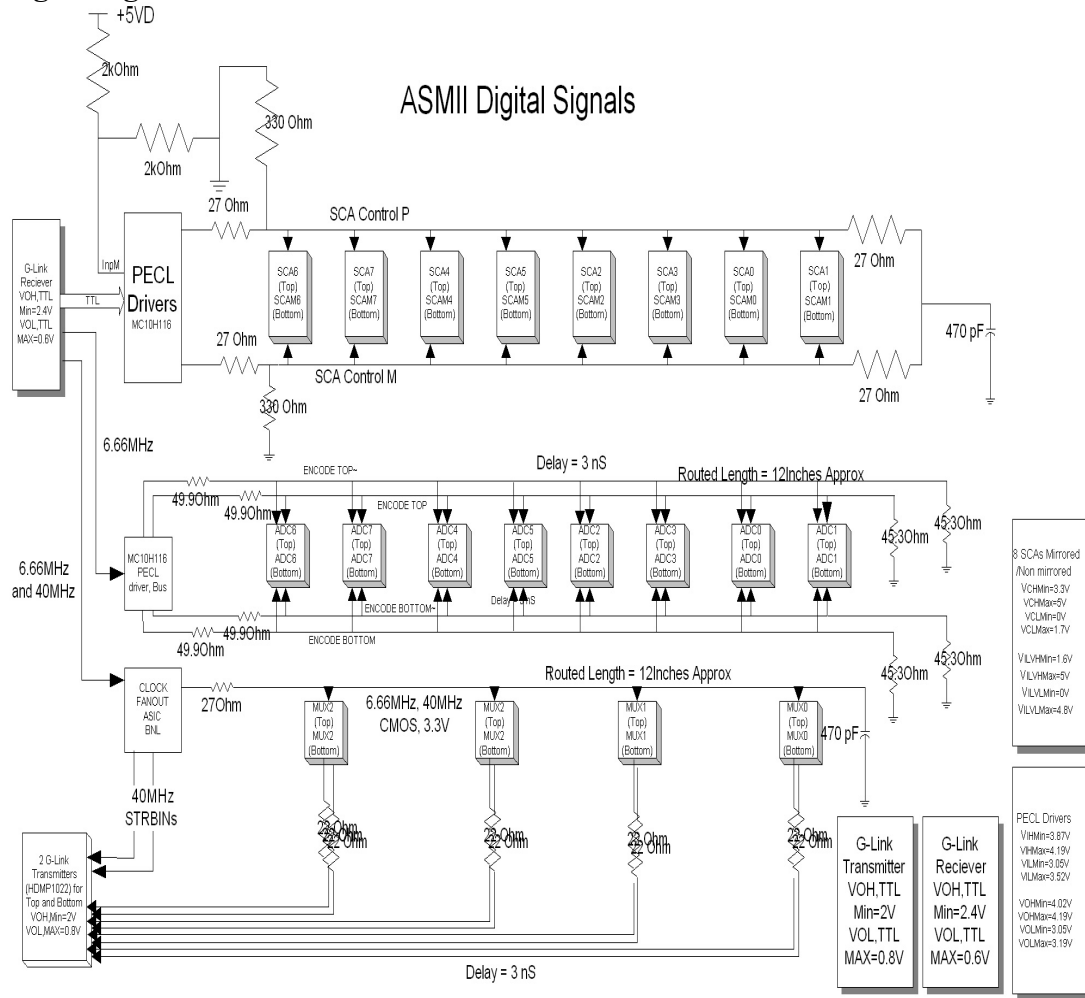
Digital signals:

Figure :3
SCA control signals and ADC clocks, ASM2MUX, G-link clocks, ASM2MUX output data run across the length of the board. These signals are treated as transmission lines. Terminations on these lines are adjusted to give right swings and minimize reflections to maintain signal integrity. SCA controls and clocks traces from the G-Link deserializer to the MC10H116 buffers are small traces, and need no terminations. The output lines driving loads of 16 SCAs are treated as differential controlled impedance lines and are terminated as such. This design is adapted from the LAr FEB. We had proposed three different clocking schemes during the CDR of ASMII and we adopt the differential clocking scheme to keep the digital swings on the board to a minimum. Group of 8 ADCs are clocked using 1 PECL buffer each. These lines are also treated as single ended transmission lines and termination resistors are adjusted to give 400mV swing centered at 1.6V.
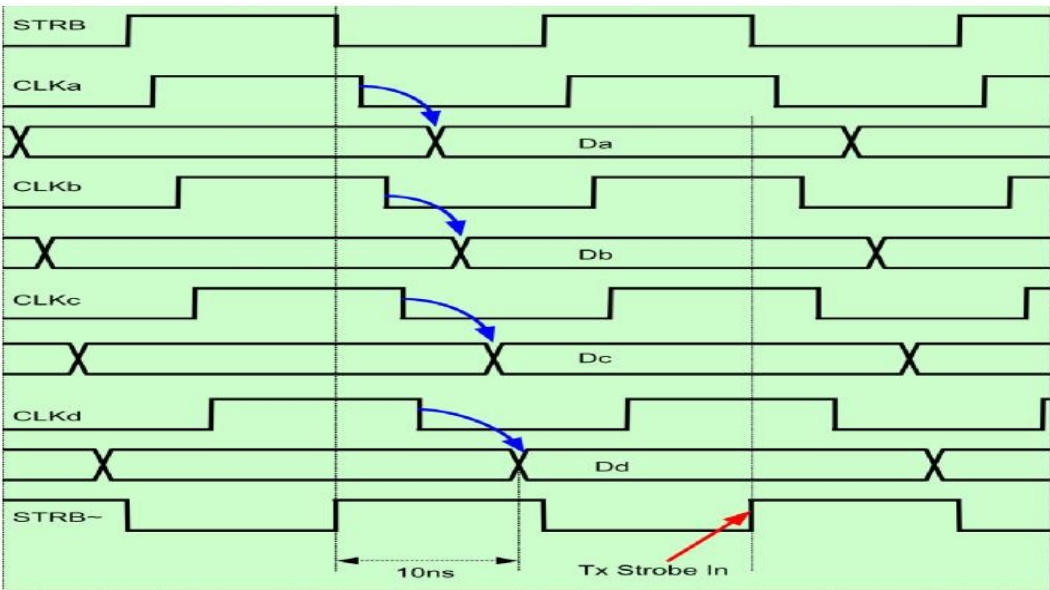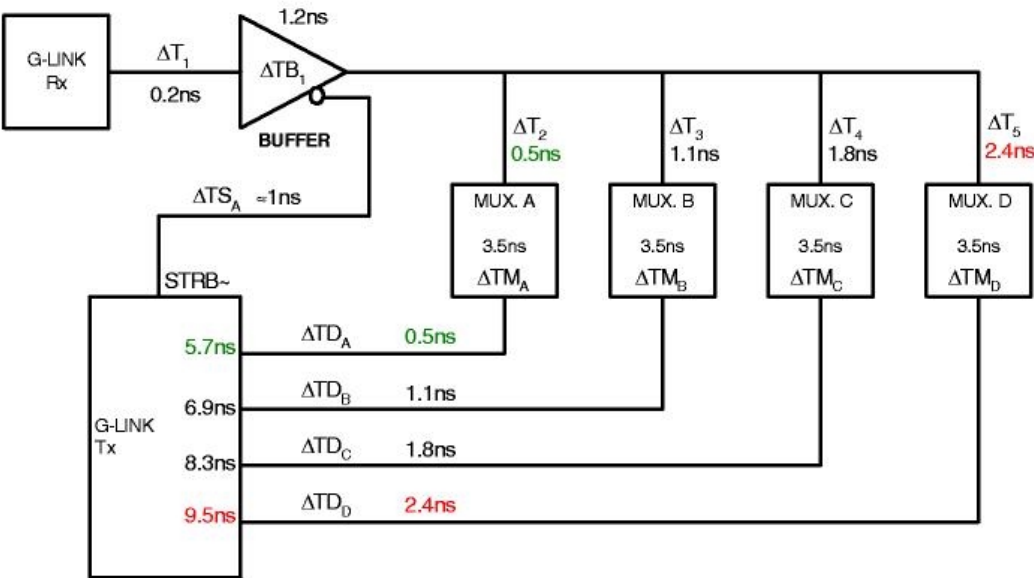
ASM2 MUX CLK/DATA Delays

Figure:4. ASMII Clocking delays.

ASM2MUX needs a 40MHz and a 6.66MHz clock. BNL Clockfanout ASIC is used to distribute clocks to 8 ASM2MUXs on ASMII. These lines have AC termination. Figure:3 shows digital signals on ASMII in detail.

STRBOUT, extracted 40MHz clock output of the deserializer is inverted inside the clock fanout chip and fed straight to the STRBIN pins of the serializer chips. This is done to account for the round trip delays of the clock and rising edge sensitive ASM2MUX outputs and meet the setup and hold times on the serializers. It gives a 12.5ns safety window, to invert the STRBIN of the G-link serializers.

ASM2MUX output data lines are different lengths depending on the location of the ASIC on the board relative to the serializer chips. These lines are back terminated using 22Ohm resistors. 4 resistor packs are used per ASIC to minimize the area and for ease of routing.

AD9042AST digital output drivers can be run off voltages ranging from 2.5V to 5VDC to suit the driven load. ASM2MUX is a 3.3V CMOS ASIC, with a logic threshold at about 2V. ADC digital output drivers are thus run of 4.1V supply, value tuned to achieve a 3.3V swing at the output. As recommended, ADC output lines have a 560Ohm series resistor, realized as an 8 and 4 resistor packs per ADC.

ASMII Power distribution:

ASMII has 7 ST LHC-4913 adjustable regulators, and power is distributed as shown in the figure:5. Analog and digital power planes are kept separate, but there's only one ground on the board.
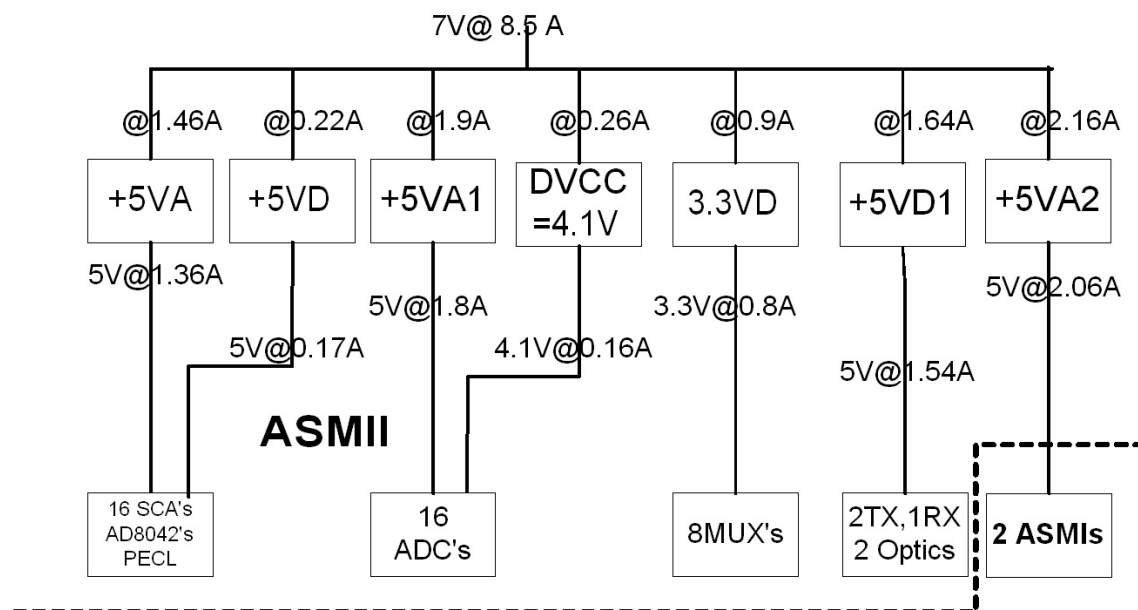
Power:
Total:59.43W

CSC ASM PACK Power
Distribution

Figure:5

Layout changes on the production version from ASMII-C:
ASMII-C is a production ready version, and needs practically no significant change but one in the layout. A series resistor of 100Ohms (Figure:1) needs to be added between SCA reference input pin and the AD8042AR output pin.

Test results:
ASMII-C has been extensively tested and characterized alone, with ASMI on a test rack and with ASMI on chamber. A system integration test was conducted at BNL with a complete set of on chamber and off chamber electronics. We present some results from this test highlighting ASMII performance. System integration test results will be presented as a separate document. The test setup consisted of 1ROD, 1 Test transition board, 5 ASMIIs, 12 ASM1s and one cathode strip chamber. ROD supported readout of 4 ASMPacks (2ASMIs and 1 ASMII).

Following figures show one of the 5 ASMPack test results. The ASMPack was numbered 5A, and was connected to bottom of layer 4 of the chamber. These results are summarized for all the 4 ASMPacks in the end.

Setup for figure 6:
Bottom 96channels of ASMII. No channel is pulsed. Reading pedestal values. 200 events with 4 samples each collected. 20MHz write, 6.66MHz read.
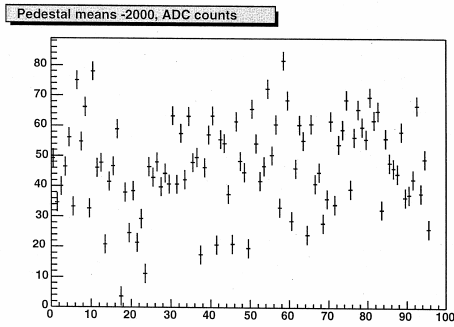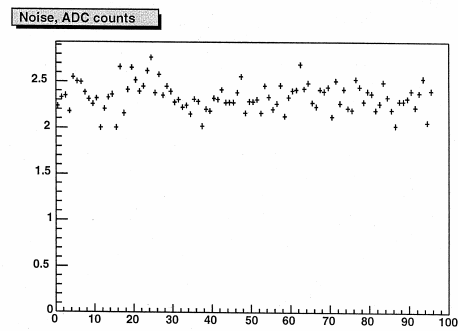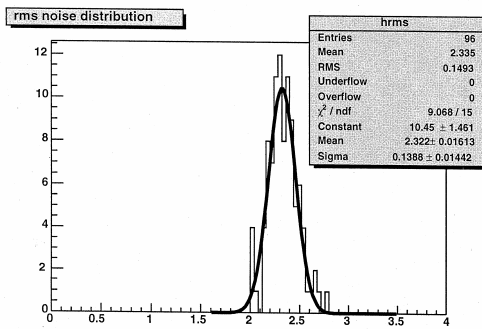
Figure 6a
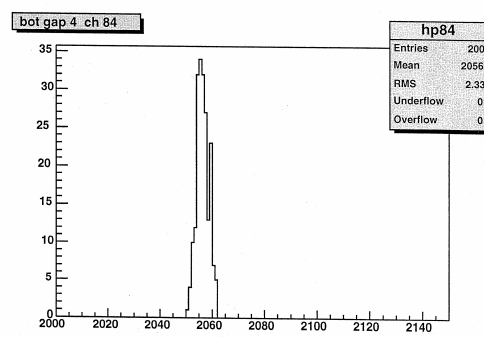
Figure 6b

Figure 6c

Figure 6d

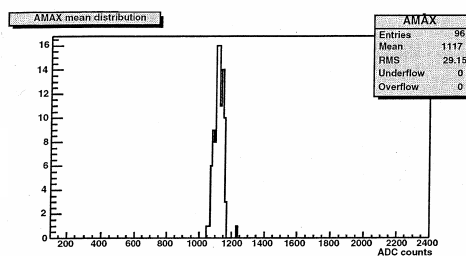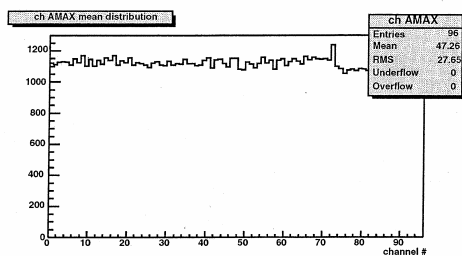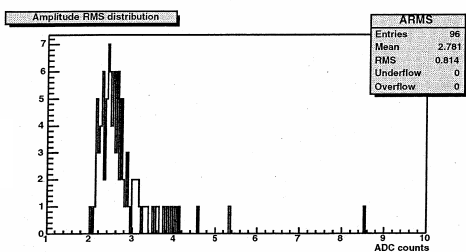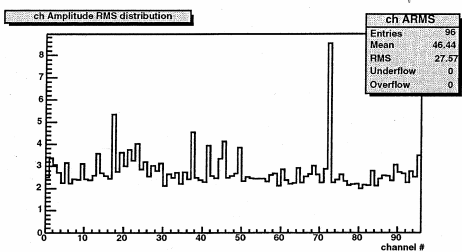| Figure 6a: Pedestal means -2000ADC counts vs 96 channels, averaged over 200 events.	Figure 6b:RMS noise in ADC counts vs 96 channels, RMS of 200 events.
Figure 6c:RMS noise distribution for 96 channels. Mean=2.335, RMS=0.1493, Sigma=0.1388	Figure 6d: Channel number 84 selected at random. Pedestal histogram for 200 events.

Figure 7a

Figure 7b

Figure 7c

Figure 7d

Figure 7e
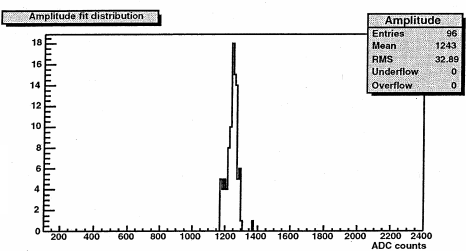
Figure 7f
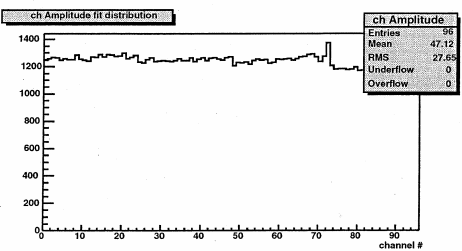
Figure 7g
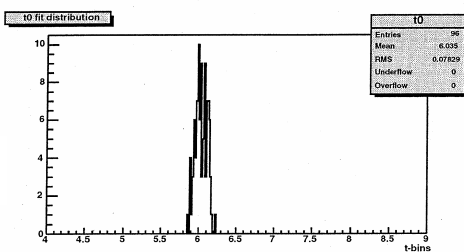
Figure 7h
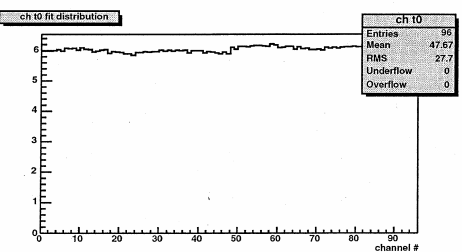
Figure 7i
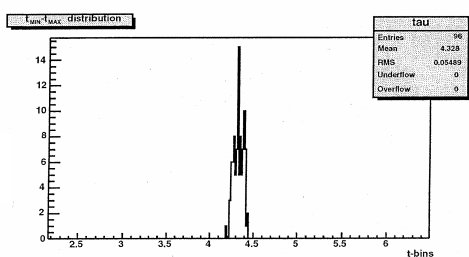
Figure 7j
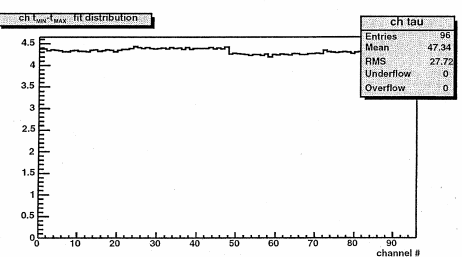
Setup for figure 6:

Bottom 96channels. All channels pulsed. 200 events with 4 samples each collected. 20MHz write, 6.66MHz read.

Figure 7a: Histogram for 96 channels, of mean of maximum (AMAX) of 4 samples over 200 events. All 96 channels pulsed together with same pulsar.	Figure 7b: AMAX mean distribution vs channel number.
Figure 7c: Histogram for 96 channels of AMAX RMS distribution over 200 events.	Figure 7d: AMAX RMS over 200 events vs channel number.
Figure 7e: Histogram for 96 channels of averages of maximum amplitudes after curve fitting for 200 events.	Figure 7f: Averages of maximum amplitudes after curve fitting for 200 events vs channel numbers.
Figure 7g: Histogram for 96 channels of averages of t0, times of occurrences of maximum in terms of 25ns time bins after curve fitting over 200 events.	Figure 7h: Averages of t0 over 200 events vs channel numbers.
Figure 7i: Histogram for 96 channels of averages of times of occurrences of minimum minus times of occurrences of maximum (tmin - tmax) in terms of 25ns time bins after curve fitting over 200 events.	Figure 7j: Averages of tmin-tmax over 200 events vs channel numbers.

AMAX mean distribution

AMAX	
Entries	96
Mean	2056
RMS	17.34
Underflow	0
Overflow	0

./ps/calibration/gap4_bot_5.ps

Figure 8a

ADC counts

ch AMAX mean distribution

ch AMAX	
Entries	96
Mean	47.54
RMS	27.66
Underflow	0
Overflow	0

Figure 8b

channel #

Setup for figure 8:

All channels pulsed, just near saturation. 200 events, 4 samples collected. 20MHz write, 6.66MHz read.

Figure 8a: Histogram for 96 channels of averages of maximum at saturation AMAXsat in ADC counts over 200 events.	Figure 8b: AMAXsat vs channel numbers.

Setup for figure 9: All channels pulsed. Calibration voltages of 200mV, 400mV, 600mV, 800mV, 1000mV and 1200mV used. 50 Events each collected for each pulse height.

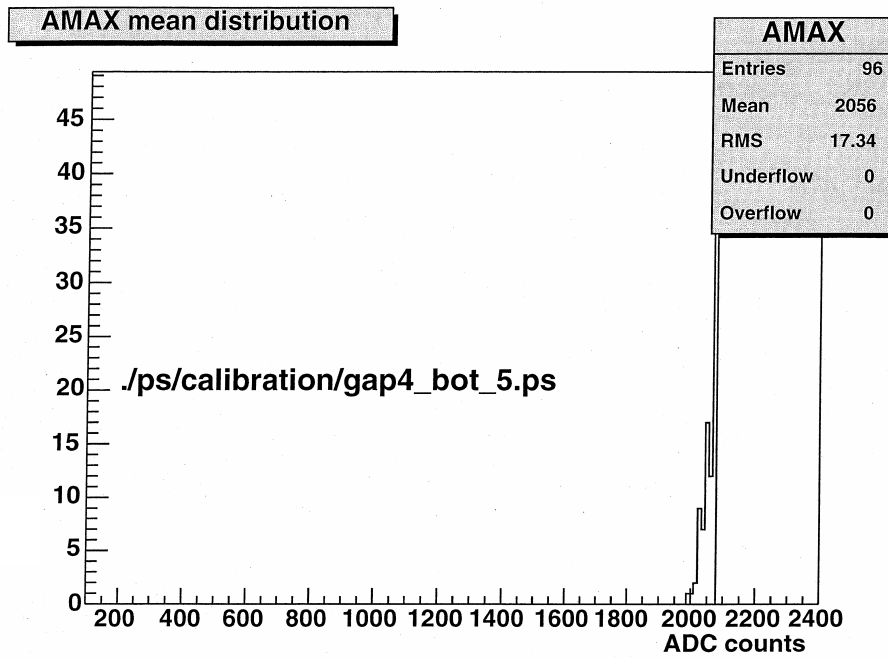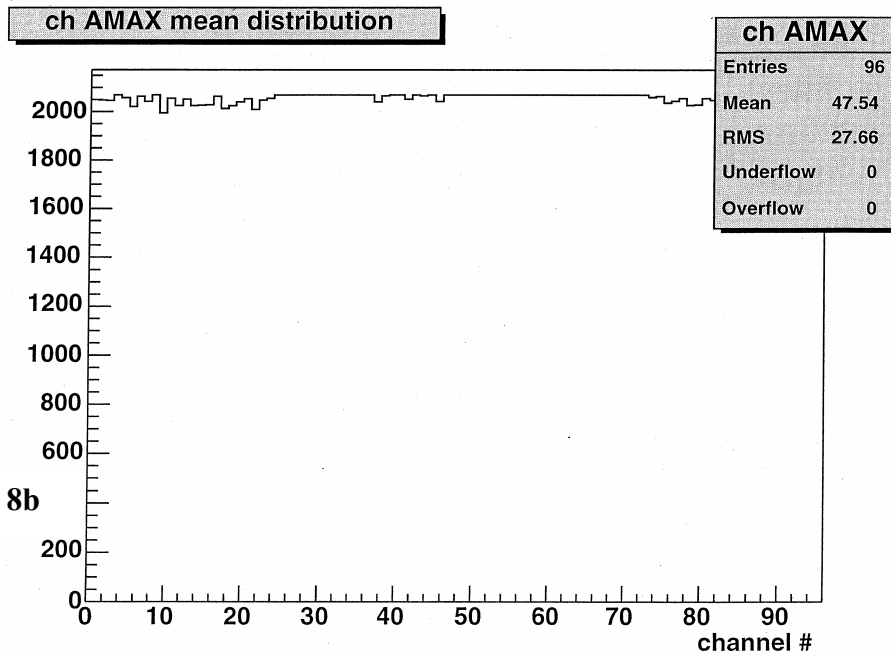| Figure 9a: Average over 50 events for 96 channels of maximum amplitude in terms of ADC counts vs input voltage to the preamps in mV.	Figure 9b: Average for 96 channels of RMS noise in ADC counts over 50 events in the maximum amplitude vs input voltage to the preamps in mV.
Figure 9c: Average time of occurrence of maximum amplitude for 96 channels over 200 events vs input voltage to the preamps.	Figure 9d: Average tmin - t max over 50 events for 96 channels vs input voltage to the preamps.
Figure 9e: Histogram of mV at the preamp output per ADC count for 96 channels.	Figure 9f: mV at the preamp output /ADC count vs channel number.
Figure 9g: Histogram for 96 channels of averages of t0, times of occurrences of maximum in terms of 25ns time bins after curve fitting over 200 events.	Figure 9h: Averages of t0 over 200 events vs channel numbers.
Figure 9i: Histogram of Y intercepts in ADC counts for 96 channels after straight line fit to the individual linearity graph like in figure 9a.	Figure 9j: Y intercepts in ADC counts for individual linearity straightline fits of individual channels vs channel numbers.
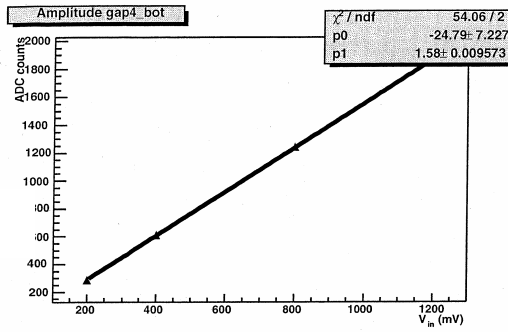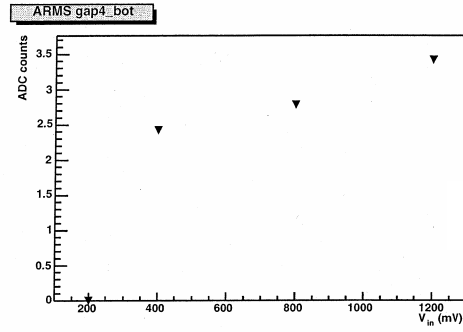
ASMII-5A

Figure 9a

Amplitude gap4_bot

χ^2 / ndf   54.06 / 2
p0   -24.79± 7.227
p1   1.58± 0.009573

ADC counts

V_{in} (mV)

Figure 9b

ARMS gap4_bot

ADC counts

V_{in} (mV)

Figure 9c

t0 gap4_bot

t-bins

V_{in} (mV)

Figure 9d

tau gap4_bot

t-bins

V_{in} (mV)

Figure 9e

k distribution

k
Entries   96
Mean   0.637
RMS   0.01636
Underflow
Overflow

mV/ADC

Figure 9f

k distribution

ch k
Entries
Mean
RMS
Underflow
Overflow

mV/ADC

channel

Figure 9g

Figure 9h

a0 distribution

a0
Entries   96
Mean   9.748
RMS   2.584
Underflow   0
Overflow   0

mV

Figure 9i

a0 distribution

ch a0
Entries   96
Mean   48.16
RMS   28.5
Underflow   0
Overflow   0

mV
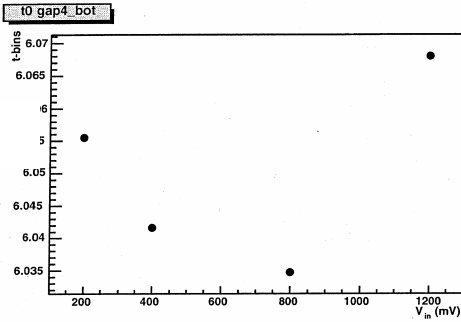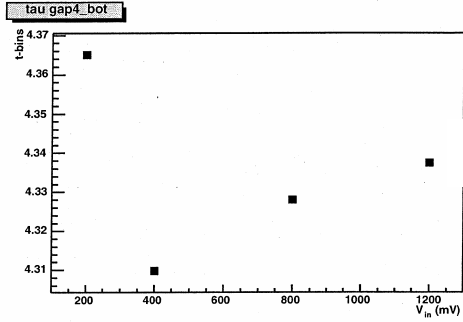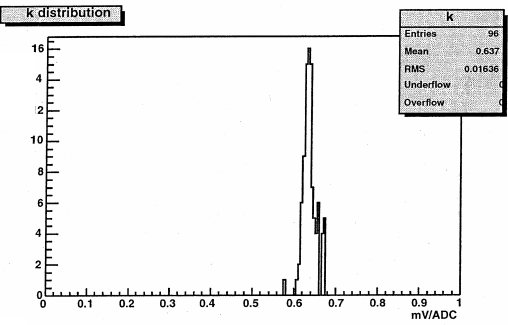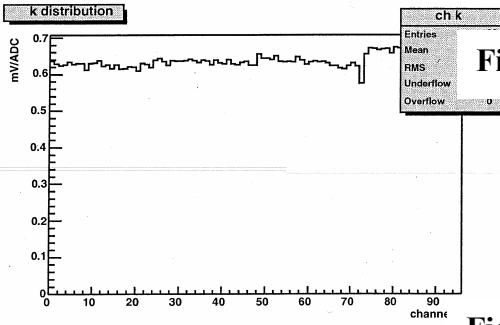
channel #

Figure 9j

ASMII number	RMS Pedestal Noise Mean in ADC Counts	Sigma	RMS Pedestal noise in electrons	Peak RMS ADC	Fit Amplitude	Channel to channel Spread	t0 /spread, 25nS time bins	ADC count/mV	Number of Bad channels
2A	2.7	0.19	2774	2.87	1260	2.10%	6.23	0.621	1
2B	2.63	0.15	2545	3.06	1336	1.30%	6.34	0.585	2
3A	2.45	0.15	2448	2.74	1297	4.60%	6.31	0.604	1
3B	2.43	0.16	2372	2.8	1343	2.50%	6.3	0.59	None
4A	2.75	0.2	2748	3.47	1298	4.00%	6.18	0.604	2
4B	2.74	0.19	2778	2.93	1259	6.80%	6.26	0.613	2
5A	2.32	0.14	2445	2.78	1243	2.60%	6.04	0.637	None
5B	2.36	0.13	2592	3	1191	2.60%	6.07	0.664	None

Summary of results for 4 ASMPacks during system integration test.

Radiation qualification of the ASICs and COTs:
Following table summarizes atlas radiation requirements:

Radiation qualification status			
COTS	Responsible	For preselection	For production
AD9042 ADC[2]	SMU	Complete	Complete
AD8042 Dual opamps[3]	Nevis	Complete	Complete
10H116 differential line driver[3]	Nevis	Complete	Complete
HDMP- 1022 serialiser[4][5][6]	SMU	Complete	Complete
HDMP- 1024 deserialiser[4][5][6]	UCI	Complete	Complete
SDX-19-4-1-S Optical Transceiver Transmitter[4][5][6]	Nevis	Complete	On procurement
SDX-19-4-1-S Optical Transceiver Reciever[4][5][6]	BNL	Now	On procurement

SDX optical transceiver is partially qualified for radiation by LAr. The receiver PIN diode needs to be tested for TID and the test setup is ready at BNL. PACRAT (PCI ASMII Control, Read out and Test) board firmware is modified to monitor link 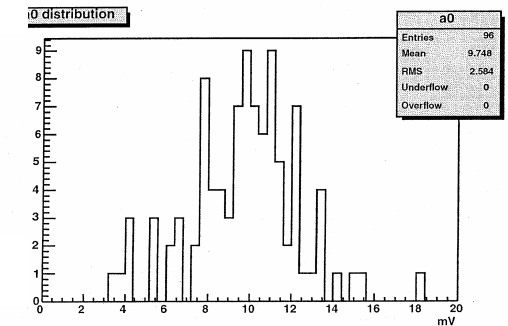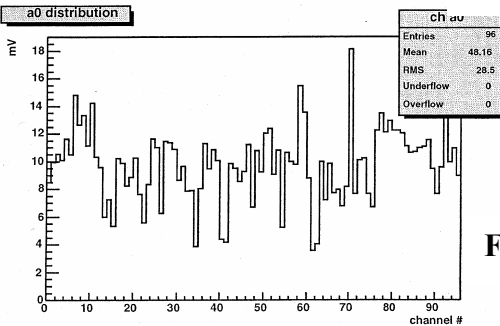loss time, SEUs, and TID tests will be scheduled at MGH. These transceivers were used during the radiation testing of the ASM2MUX, and were in the close proximity of the proton beam (less than 5 inches). Total of 5 ASM2MUX devices were tested, and the optical transceivers remained unchanged during swapping of these devices. Transceivers seemed to have weathered rates which can be compared to Atlas enviornment. Although this doesn't rule out the radiation testing for these components, it gives an impression that they will qualify and link loss times will be within acceptable limits.

Two of the ASICs used on ASMII, HAMAC Muon SCA, ASM2MUX radiation qualified and production is complete. Clock fanout is a simple chip using the same standard cells, IO pads and package as ASM2MUX is designed in the HP 0.5u process. We conclude from the radiation test results of testing done on ASM2MUX, Preamp shaper chips that HP-0.5u process can sustain the radiation dose over the LHC experiment. It can further

be argued that clock fanout chip used on ASMII be regarded as rad-tolerant by virtue of the process and its simple and similar design as already qualified ASM2MUX.

Production plans:

Procurement:

Following table lists the lead times and cost estimates on the components needing procurements:

There will be 5 ASMII Boards per chamber and 32 chambers								
Total of 180(160+20)ASMII Boards with 192 channels per board								
			180		boards			
Part Number	Description	Manufacturer(/Vendor)	Qty/ASMII	Production Qty	Unit Cost	Production Cost/ASMII	Production Cost	Approximate Lead time
HDMP-1022	Serializer	Arrow	2	360	$52.75	$105.50	$18,990.00	4-6weeks
HDMP-1024	Deserializer	Arrow	1	180	$52.75	$52.75	$9,495.00	4-6weeks
MDX-19-4-1-8	850nm optic tranciever	Stratos Lightwave	2	360	$73.00	$146.00	$26,280.00	8-10weeks
1711084	Conn TERM blocks	PHOENIX Contact	1	180	$3.00	$3.00	$540.00	1week
1-77984-0	Conn to ASM1	AMP	2	360	$10.00	$20.00	$3,600.00	1week
Passives	Passives	Digikey	1	180	$100.00	$100.00	$18,000.00	1week
Total Material Cost						$427.25	$76,905.00	$76,905

Following table shows production timeline. Assuming fabrication purchase order is sent out on July1, 2004, we believe, production and testing of ASMII will be complete by October 29, 2004.

ASMII Board production timeline			
Task	Duration Days	Start	Finish
Fabrication Start	25days	1-Jul-04	26-Jul-04
Parts procurement & kit preperation	34days	1-Jul-04	4-Aug-04
SDX Transciever radiation testing	1day	TBD	TBD
SDX Transciever procurement	56days	1-Jul-04	26-Aug-04
Assembly Start	28days	27-Jul-04	24-Aug-04
Mount SDX Transcievers	5days	25-Aug-04	30-Aug-04
Recieve 1st articles	14 days	27-Jul-04	10-Aug-04
Evaluate 1st articles	7days	8-Aug-04	15-Aug-04
ASMII Board testing	60days	30-Aug-04	29-Oct-04

ASMII fabrication:
Board size: 17.125" x 4.804"
Surface Finish – Electroless Ni, Immersion Au
2,907 Holes, smallest hole 0.016" dia
Test Points - 2,325
Line Width & Spacing, 0.006" & 0.006"
Ten (10) Layer, Tetra II Hi-Temp Epoxy 0.072" Thick
25 days for fabrication of 180 boards.

Assembly:
All components will be mounted and trimmed to IPC 610. BNL to supply CADD files. Total of 180 ASMIIs are needed for the full scope of CSCs. First article of 10 will be produced first and tested. The rest of the 170 boards will be assembled and received in batches, last batch expected in the week of 22nd Aug, 2004.

QA and QC:
Visual inspection will be conducted by the assembler and possibility of electrical tests is investigated. Before powering on, each board will be tested for possible shorts between GND and between power planes with a multi-meter. After passing this test, the board will be powered on the bench without plugging on to the test rack of well characterized ASMI. The power supply will be current limited to 9Amps. On a successful power up without any current overdraw, the board will be powered down and plugged on to the rack. A pedestal run will be conducted and 500 triggers at 25 samples and latency of 1us will be taken and written to the disk with the board ID. Board will be provided with a bar-coded ID in compliance with the CERN standard. Data from the pedestal runs will be written. Pedestal run file will consist of following information:

Baseline, average, RMS noise. Following channels will be flagged:

1]Any channels with higher than 3ADC counts(ENC>3100e-)
2]Channels baseline variation greater than 10% of the baseline
3]Any ADCs, ASM2MUXs with stuck bits.

Then all the 192 channels of the board will be pulsed using pulsar board which can in principle select any random combination of the 192 channels and pulse at any given amplitude between 0 to 2V in the steps 200mV, starting at 200mV up to 2V and the, 50 triggers at each level will be recorded at window sizes of 25 samples and 4 samples. Reconstruction algorithm will be run on the acquired data and statistics presented for ASMII-5A will be recorded for each channel and will be stored. Dead channels will be flagged. The board will brought back to instrumentation division for repairs if needed. Detailed description of the test setup is presented later.

Following table lists errors observed and corresponding fixes.

Symptoms	Possible reasons in the order of decreasing probability	Cure
Dead	1]Ripped pin from the surface mount	Resolder the pins, change the

channels	connector between ASMI and ASMII 2]cold solder pins on SCA	connector if needed
Stuck bits	1]Visual inspection of the resistor packs. 2]Loose, shorted AD9042 output pins 3]Loose, shorted ASM2MUX output pins 4]Loose, shorted HDMP1022 input pins	Resolder pins, change resistor packs.
High noise	1]Grounding strips on the chamber 2]Cold solder joints on the SCA bias pins	Add more grounding strips between different layers.
Baseline shifts	1]Check for the resistor values setting the gain for the differential amplifier	Change the resistors to right values

Burn in:

Tested and accepted boards will be burned in on the chamber together with ASMI as a pack, for 168hours at a stretch, and screened for failures before mounting on the chamber.
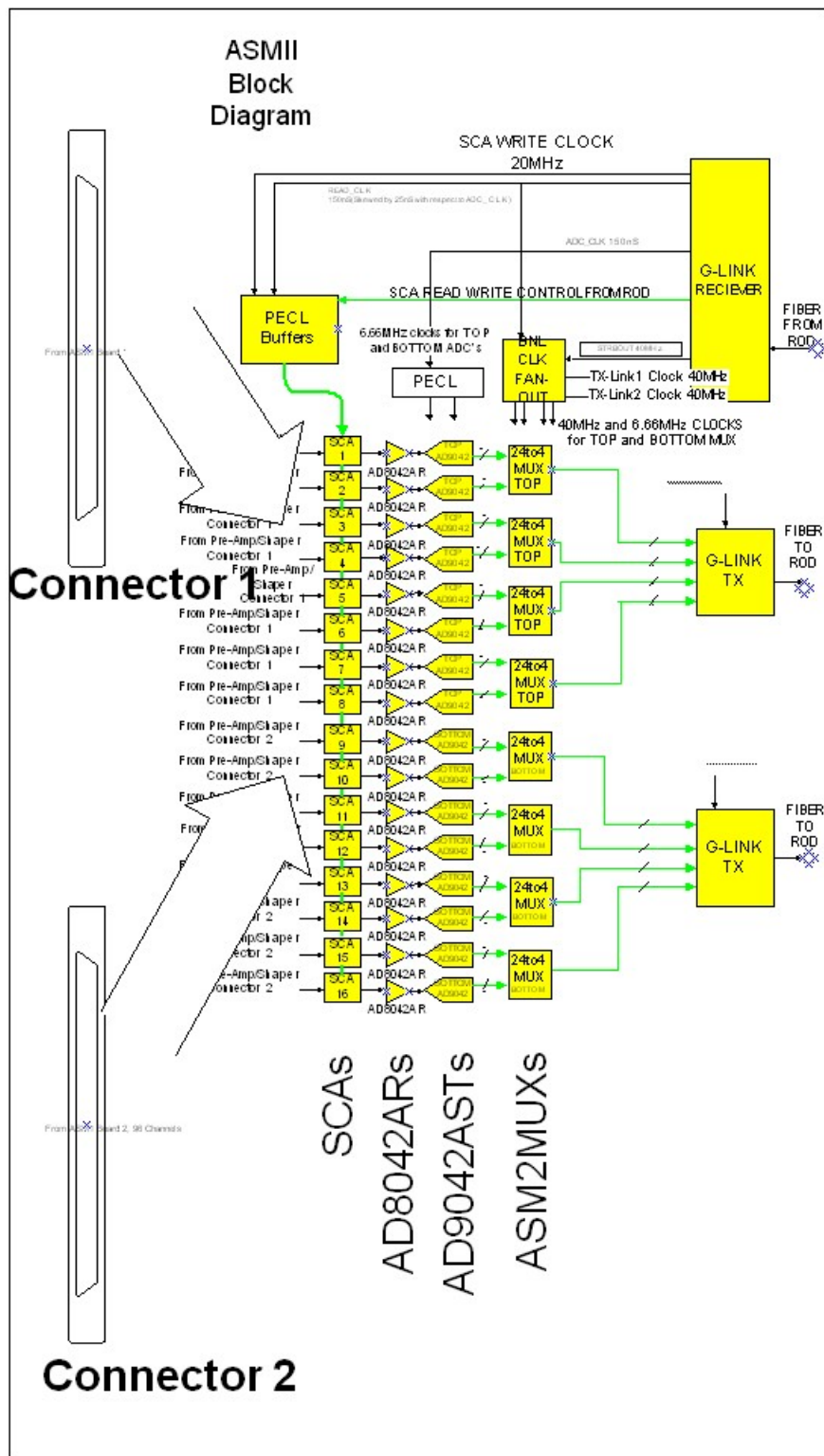
Figure:10 ASMII Block Diagram

ASMII Testing:
PACRAT:

      PACRAT is a custom designed PCI board designed at BNL. It contains 2 G-Link receivers, 1 G-Link transmitter, 1 Lemo connector for asynchronous trigger input, and Altera EP20K400 FPGA which acts as a PCI interface controller as well as ASMII Controller. PACRAT transmits control signals to and receives data from one ASMII on a giga bit optical link. It accepts an asynchronous TTL trigger input on the Lemo cable. It can support data transfer rates upto 70Mega Bytes per second, from its on board memory to the PC via PCI interface.

Figure 11: PACRAT Block Diagram

SCA Control:

      SCA Control algorithm resides on the Altera FPGA on PACRAT. Following flowchart illustrates the algorithm.

ASMII SCA Controller Modes:
(Simultaneous read and write.
      OR
Sequential read and write)
      AND
(40MHz SCA Write Clock
      OR

20MHZ SCA Write Clock)
                AND
(6.66MHz SCA RD Clock, ADC_CLK, MUXSCLK
                  OR
 5MHz SCA RD Clock, ADC_CLK, MUXSCLK)

Figure :12 ASMII SCA Control Algorithm
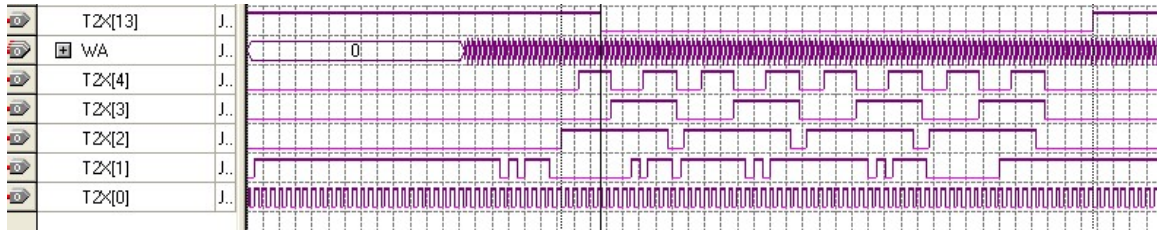
Figure:13 SCA Control simulation

Above figure shows functional simulation of ASMII SCA Controller on PACRAT. Four memory locations (window size = 4) from the SCAs are read out, with a latency of 40. Latency is equal to time delay in the occurrence of the trigger and its propagation to PACRAT, and then down to ASMII, rounded off to nearest integer number of SCA write clocks. Presumably the triggered data (pulse) is found in a window starting at this location.

Existing ASMII Test system designed at BNL consists of one 1 to 8 fanout NIM module for pulsing, two backplane trigger 4 to 96 fanout boards, 2 fully tested working ASM1 boards, 1 PACRAT (**P**CI **A**SMII **C**ontrol, **R**eadout **A**nd **T**est board), one Intel P-IV PC running windows XP and a software GUI written in C++ and NI Labview.
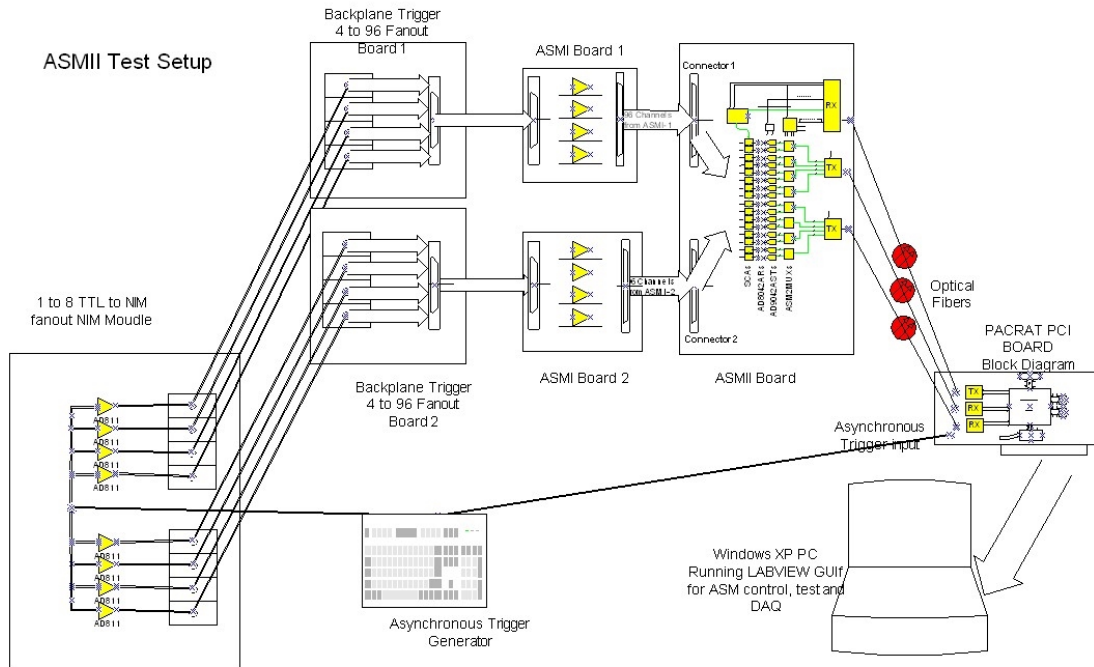
Figure 14: ASMII Test Setup

Noise measurement setup:
No ASMII Channels will be pulsed during noise measurements. Only pedestal values at the SCA inputs will be read for a given trigger. Following readings are with the simultaneous read write, 20MHz write clock and 6.66MHz read clock. For each trigger, 25 SCA Samples were read out from the SCA pipeline. Total of 1000 samples were collected per channel, over 40 triggers to get the statistics in Figure 7a and 7b. The

statistic was updated for every new trigger worth of data. To summarize, the average RMS Noise found on board was 1.89 ADC counts.

Functionality Test:
All the 192 ASMII Channels will be pulsed simultaneously, and the pulses will be reconstructed using Labview program for real time viewing. Data will also be written to a file for similar root analysis as presented for ASMII-5A.
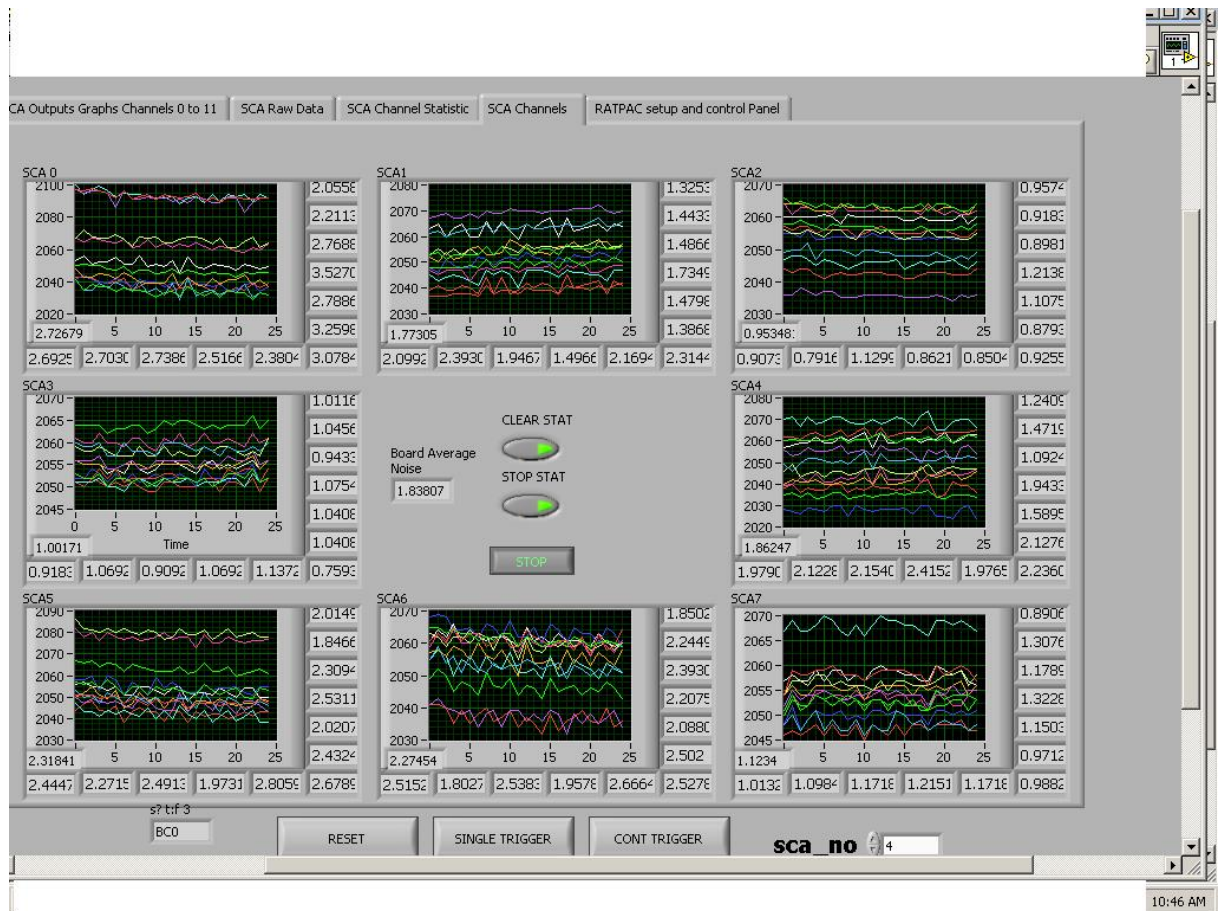
Figure 15: RMS Noise on 96 Top Channels, Average Noise per SCA, Average noise for the bottom half of ASMII.
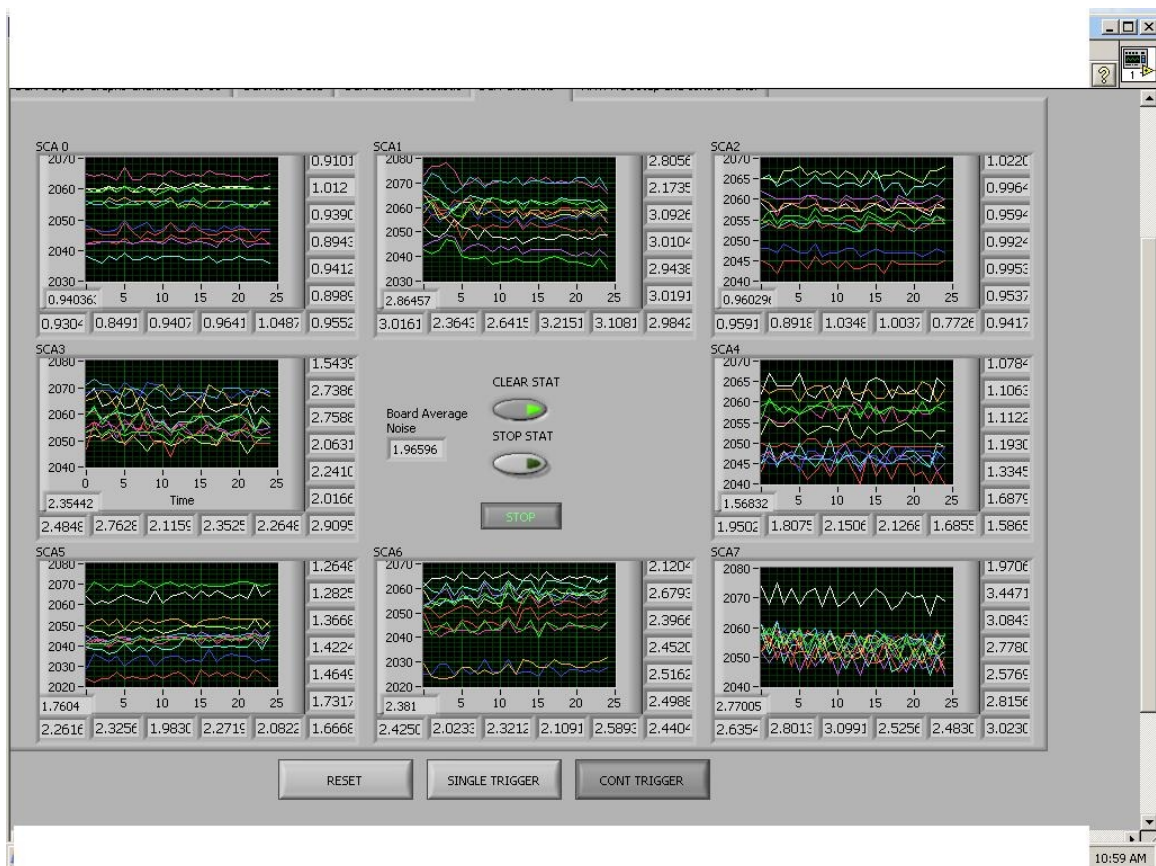
Figure 16: RMS Noise on 96 Top Channels, Average Noise per SCA, Average noise for the top half of ASMII.
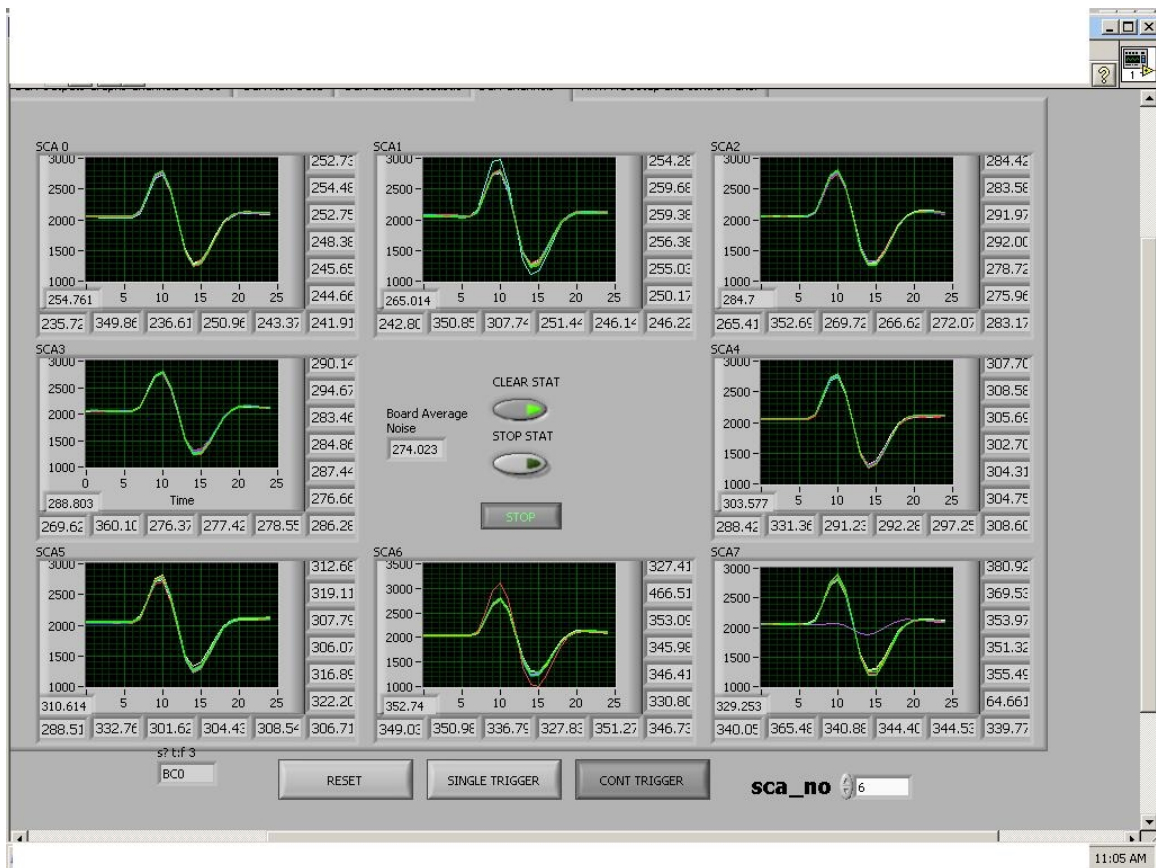
Figure 17: Top 96 ASMII channels pulsed. Window size 25.
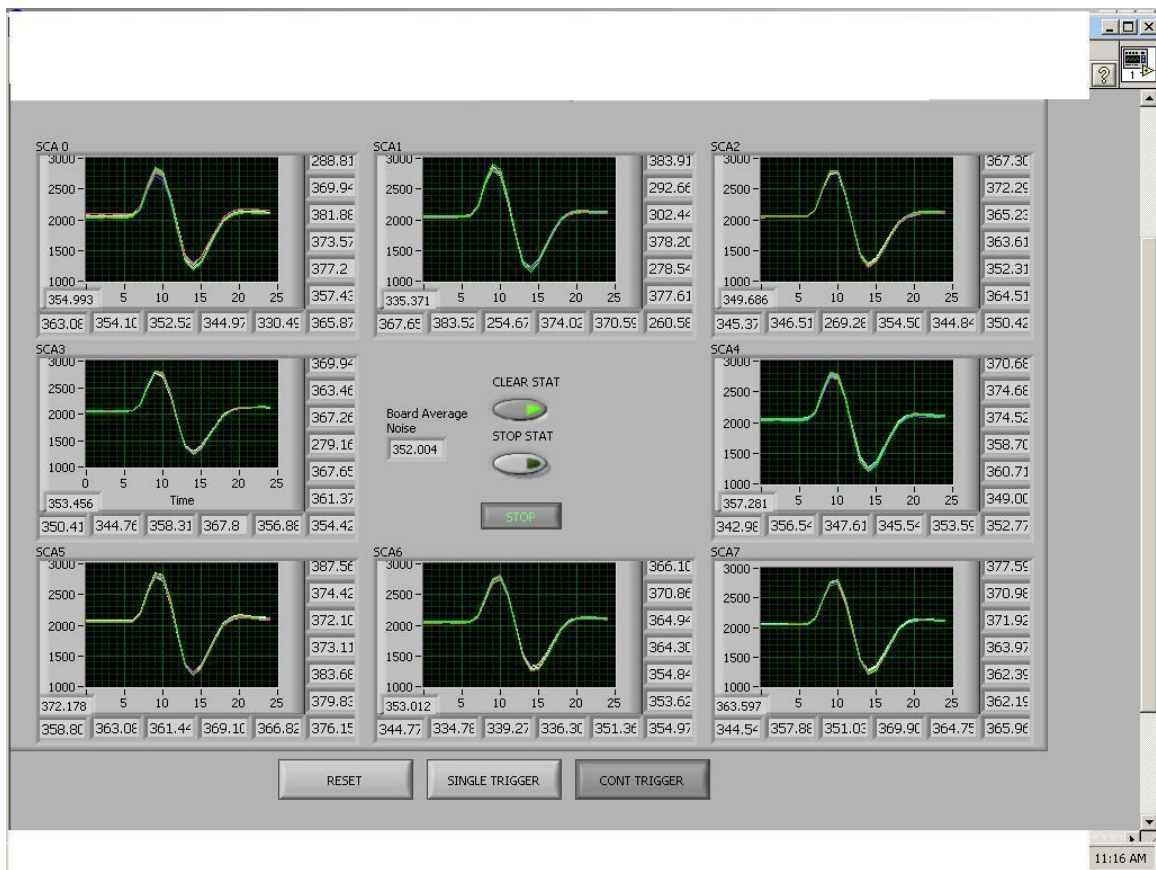
Figure 18: Bottom 96 ASMII channels pulsed. Window size 25.

Conclusion:

ASMII board for CSC electronics has evolved through 3 iterations. All the design issues have been addressed on the final production ready version of the board, ASMII-C. The board needs just one minor layout change. Its performance at the system integration test was excellent, and meets all CSC specifications such as noise, cross talks and trigger rates. All the COTs and ASICs have been tested for radiation, except for the PIN diode in the optical receivers. PACRAT firmware has been modified and system for radiation testing of the optical receivers is ready. Test procedures, quality assurance and control plans have been chalked out and ASMII board is ready for production.

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[6] M.L. Andrieux b "Development of radiation tolerant Gb/S optical links for the front end read out of the Atlas Liquid Argon Calorimeter."

Performance and Radiation Tolerance
of the ATLAS CSC On-Chamber Electronics

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Abstract

The on-detector electronics for the ATLAS Cathode Strip Chamber (CSC) performs amplification, analog buffering, and digitization of the charge signals from individual cathode strips. Working in a high-rate environment (strip hit rate up to several hundred kHz) the system requires a signal-to-noise ratio of 200:1 and a minimum dynamic range of 10-bits. The implementation of the on-chamber electronics to meet the CSC requirements is described, along with a discussion of the proposed system architecture and how it minimizes the problem of radiation induced errors and failures.

I.   Introduction

The CSC system forms the forward section of the muon spectrometer of ATLAS. It consists of 64 chambers. Each chamber consists of four layers. There are 768 precision (x) and 192 (y) strips per chamber. The readout pitch is 5.547mm. Strip capacitance is 20-50pF. Interpolation is performed only on the precision strips. Front end electronics are located on ASMI and ASMII boards within Faraday shields along the narrow edges of each chamber, as
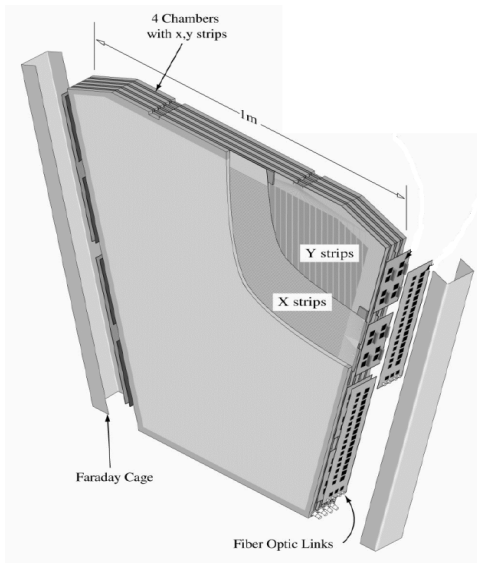

Figure 1. CSC Chamber

shown in Figure 1. Each chamber consists of ten ASMI assemblies and five ASMII assemblies. Transition boards provide shielding and optimal mapping of signals between the preamplifiers on the ASMI and the sampling and digitizing functions on the ASMII. .

There are eight ASMI assemblies and four ASMII assemblies dedicated to the precision strips. Two ASMI assemblies and one ASMII assembly service the transverse strips.

The outer skin of the chamber is ground. A continuous strip of copper exists around the perimeter of the cathode planes to connect to the skins. The purpose is to provide a low impedance connection at all points on the chamber. The Faraday shield is connected to the chamber by bolts. These bolts also serve as ground connection point to the skin and provide a connection within the Faraday shield to the circuit boards. Low voltage, +6VDC is brought to the circuit boards from a remote power supply via bulkhead terminals. Three multimode fibers are connected to the ASMII via SC bulkhead fiber connectors. Bulkhead connectors are used to maximize the effectiveness of the Faraday shield.

The ASMI assembly consists of eight custom CMOS preamplifier-shaper ICs [2] with 12 active channels and one reference channel. for coherent noise reduction.

The ASMII assembly stores analog samples, digitizes the samples to 12-bits then serializes the ADC data to two gigabit optical links to the off-detector electronics. Control to the sampling and digitizing circuitry is provided via fiber optic link from the off chamber electronics.

II.   System Architecture

The ATLAS CSC system architecture is illustrated in Figure 2. Charge from ionized gas induced on the cathode strips is amplified on the ASMI module by the preamp shaper. Bipolar 7th – order shaping is performed. Twelve active channels are used. The twelve signals along with a reference signal are sent to the ASMII via the transition board. These signals are connected directly to the a custom CMOS switched-capacitor analog memory (SCA) [1]. The SCA consists of an array of 12x144 storage cells with simultaneous read-write capability. Control of the SCA is. sent over an Agilent Technologies G-Link optical link operating in the single frame mode with a 20-bit data field operating at an 40MHz frame rate.
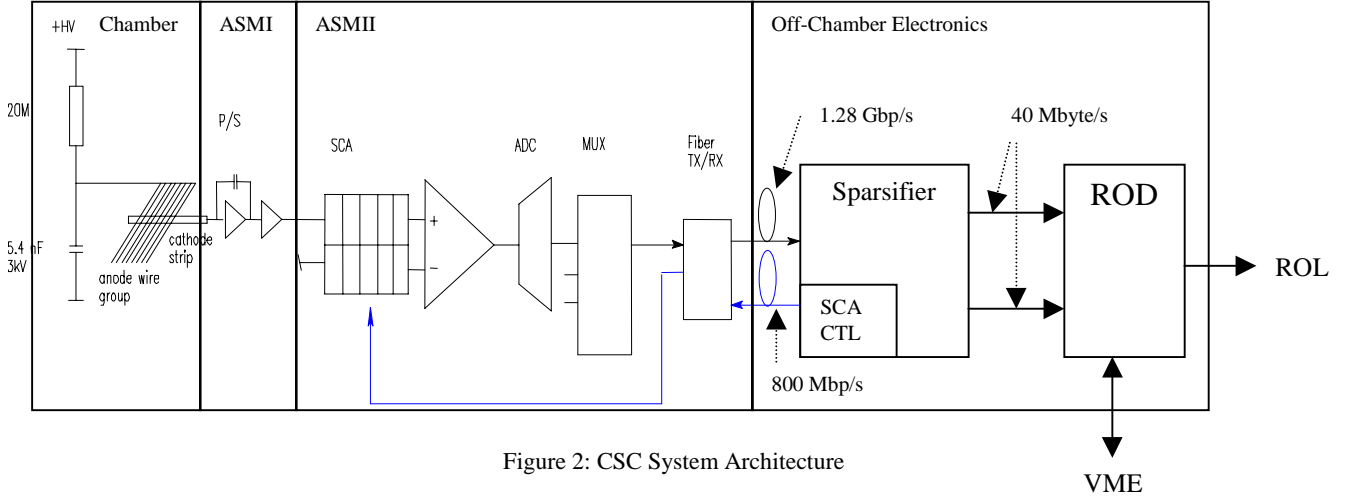
Figure 2: CSC System Architecture

Data is transmitted from the ASMII over two G-Links to the off-chamber electronics at a rate of 640 Mbp/s per link or 1.28 Gbp/s total. The aggregate chamber rate is 6.4 Gbp/s. There are two end-caps with each end-cap consisting of 32 CSC chambers. Total data rate per end-cap is 206 Gbp/s or 412 Gbp/s for the entire CSC system. Each of the "downstream" G-Link data links operate in the 16 bit single frame mode with a frame rate of 40MHz. Only raw data is transmitted from the chamber. When a trigger is received the off-chamber electronics initializes the SCA read, only at this time is meaningful data transmitted. Between triggers the G-Link transmits fill frames to maintain link synchronization.

III. Signals and Noise

Muons generate about 75 electron-ion pairs (Landau peak). About 12% of charge is collected by the precision cathode in 100ns. The average signal size expected is 144fC where the central strip of the cluster receives approximately half of the charge or 72fC. The electronics noise should not degrade the position resolution of the system. The required input referred noise as a function of the average charge is calculated by the following expression:

$$\sigma_{x,elec} = \frac{\sqrt{3} \cdot d \cdot ENC}{Q_\lambda} \le 33 \mu m \qquad (1)$$

Where d = strip pitch, ENC = equivalent input noise charge, and Q_λ = total charge induced on cathode plane. From this expression the the calculated required noise limit is:

$$ENC \le 0.5 fC = 3100 e^- \leftarrow Total\ input\ referred\ noise \quad (2)$$

The required signal to noise ratio is calculated as:

$$SNR_{max\ strip} = \frac{Q_{\lambda,cent}}{ENC} = \frac{72 fC}{3100 e^-} = 145 \qquad (3)$$

The dynamic range required for a 98.5% efficiency is calculated as follows:

$$\frac{Q_{fs}}{Q_\lambda} \ge 5, \quad \therefore Q_{fs} \ge 5 \cdot Q_\lambda = 725 \cdot ENC \cong 360 fC \qquad (4)$$

where Q_{fs} is the full-scale charge. Preamp/shaper gain for V_{FS} (positive lobe of bipolar waveform) is defined as:

$$P/S\ Gain = \frac{V_{FS}}{Q_{FS}} = 4.7 mV / fC \qquad (5)$$

Quantization noise as a function of the full-scale charge and total input referred noise can be calculated by:

$$\frac{Q_{FS}}{2^{Nbits} \cdot \sqrt{12}} << ENC \quad \therefore Nbits >> 7.7 \qquad (6)$$

To minimize the quantization noise of the ADC such that the predominant noise source is the preamp/shaper an Analog Devices AD9042 12-bit ADC has been selected. Concern over gain and offset variations as well as exposure to radiation was also a criterion for this selection.

IV. High Rate Performance

The ATLAS muon CSC is subject to a high background rate environment. The overall background rate expected is 10^7 Hz per chamber. Background consists of 50% charged particles, 50% neutron and γ. Charged particle background is rejected by a timing window around trigger or by pattern recognition of non-projective tracks. Out-of-time background suppression is performed off-chamber in the Sparsifier, neutron rejection is performed off-chamber in the ROD or offline.

Neutral particles produce short-range electrons that are generally confined to only one layer. However, neutrals that hit anywhere in the chamber induce charge on all strips by anode-cathode crosstalk defined as:

$$Q_{cross} = \frac{C_{ac}}{C_{filt}} \cdot Q_{anode} \cong 10^{-4} Q_{anode} \qquad (7)$$

where C_{ac} is the capacitance from a strip to the anode wire ($\sim$ 0.5 pF), and C_{filt} is the high voltage filter capacitance ($\sim$ 5 nF). Some of the neutrals can produce very large charges:

- 50% of neutrals above Q_{FS}
- 1% of neutrals above $6 * Q_{FS}$

The cumulative result of this induced charge on all of the strips behaves like electronic parallel noise, thereby degrading both the position resolution and efficiency of the chambers

IV.   Sampling

The number of waveform samples that can be transmitted off detector is limited by the optical link bandwidth. Because of the 35 ns maximum drift time of the CSCs, it is impossible to select a set of four samples at 40 MHz that guarantee inclusion of at least one sample before and after the peak of the preamplifier waveform (see Fig. 3 below).
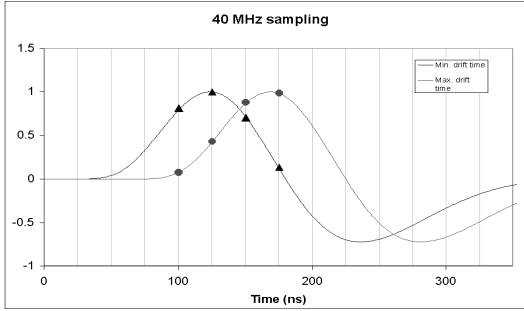
Figure 3.   40 MHz Sampling

The L1 trigger incurs a latency that includes cable delay and electronics processing by the TIM module and the off-chamber back of crate cards. This latency is estimated to be 98 bunch crossings. Additional latency is incurred by signal propagation from off-chamber to on-chamber electronics and the readout latency of the SCA. An additional 27 bunch crossings is estimated for this latency. The total estimated latency is 125 bunch crossings. The worst-case latency condition occurs for the maximum L1 trigger burst rate defined as eight consecutive triggers each spaced at 125ns intervals. The SCA is read-out at a rate of 6.67 MHz (150ns). Since 15 clock cycles are required to readout one time sample the 8th trigger arrives before the first time sample of the first trigger is readout. Beam studies have indicated that four time samples are adequate. The pipeline depth required for eight triggers would then be 32 bunch crossings. The pipeline depth of the SCA is 144 bunch crossings. Since the L1 trigger latency has been estimated as 125 bunch crossings and the required pipeline for an

eight trigger burst is 32 bunch crossings the SCA pipeline depth of 144 bunch crossings is not adequate. To circumvent this problem we have chosen to sample at a rate of one-half the bunch crossing rate or 20 MHz. Figure 4 illustrates the case of 20 MHz sampling. Again two waveforms are shown to illustrate the maximum drift-time of 35ns; now the peak and its neighbors are selected for the worst-case drift times.
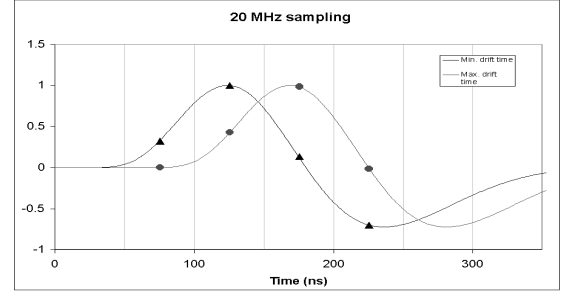
Figure 4.   20 MHz Sampling

The SCA pipeline depth is effectively doubled to 288 bunch crossings. Studies of existing beam test data were analyzed by decimating the 40 MHz sampled data by a factor of two. Decimation was done for both even and odd samples. The result of the analysis indicated no increase in inefficency.

V.   Preamp/Shaper and ASMI

Each ASMI contains eight preamp/shapers supporting a total of 96 channels per ASMI. Each ASMI contains edge connectors that directly plug into cathode plane fingers that protrude from the chamber. On each side of the chamber four ASMI modules pick up two planes.

The Preamp/Shaper ASIC has been fabricated in a 0.5 μm CMOS technology. Table 1 summarizes the measured characteristics of the preamp/shaper ASIC [2].

Technology	0.5 μm CMOS
Channels	16
Die size	2.78 x 3.96 mm
Architecture	Single-ended
Intended Cdet	20 – 100 pF
Input device	NMOS W/L = 5000/0.6 μm, Id = 4mA
Noise	1140 + 17.6 e-/pF
Gain	3.8 mV/fC
Max. linear charge	450 fC
Class AB Output swing	To power supply - 250 mV
Pulse shape	7th order complex Gaussian, bipolar
Pulse peaking time, 5% - 100%	73 ns
FW1%M	340 ns
Max. output loading (3% distortion)	500 Ω, 500 pF
Crosstalk	0.8% adjacent, 0.5% non-adjacent channel
Power supply	Single +3.3V
Power Dissipation	32.5 mW/chan

Table 1.   Preamp/Shaper Specifications

Figure 5. ASMII

VI. ASMII

All on-chamber signal processing excluding pre-amplification and shaping is performed on the ASMII. Each ASMII is capable of processing 192 channels. There are four precision ASMII's and one transverse ASMII per chamber. Signals from the preamp/shaper are sent to the ASMII from the ASMI through a transition board. Each preamp transmits 12 channels and one reference channel to each SCA. The purpose of the reference channel is to subtract coherent front end noise at the output of the SCA. The ATLAS LAr Calorimeter SCA has be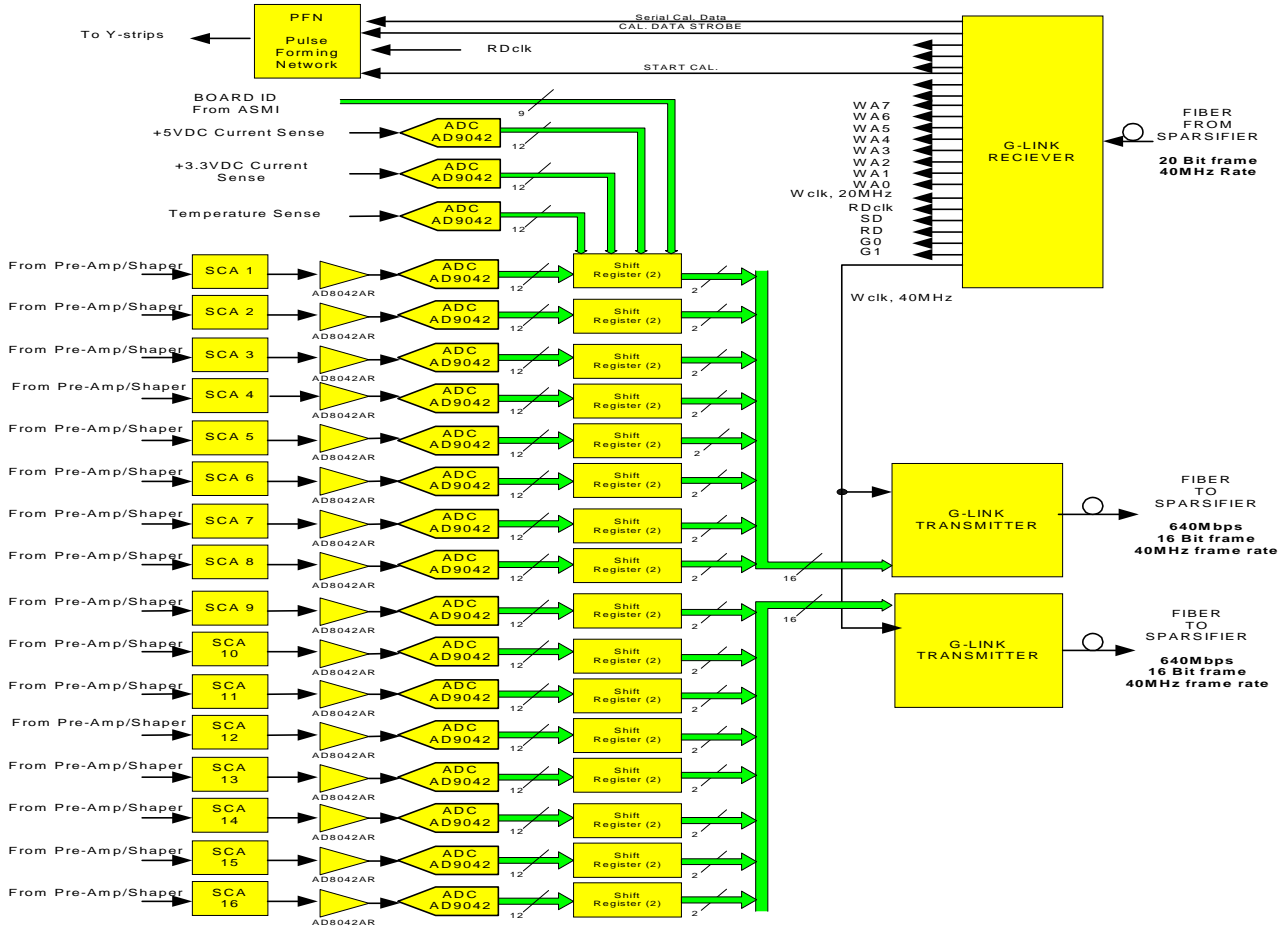en modified for use in the muon system. By applying the correct voltage to a dedicated pin on the SCA operates in muon mode where cell's are continuously read-out to a dedicated ADC. The SCA outputs are then quantized to 12-bits by Analog Devices AD9042 ADC's. Each 12-bit ADC output is split into two 6-bit data streams that are converted to serial data at 40MHz bit rate. COTS shift registers will be used for this application. Each ADC then occupies two data lines of the G-Link serializer. The G-Link transmitters are configured to operate with a 16-bit input word in the single frame mode at a frame rate of 40 MHz. There are two optical transmitter links, each link supports data transmission of eight ADC's. Four additional parameters are transmitted. Board ID is a hard-coded address corresponding to the physical location of each ASMII. Current sensing resistors will monitor the ASMI +3.3VDC and ASMII +5VDC supply currents. Temperature will be monitored on the ASMII. Each of these parameters are transmitted by streaming the digitized word of into two unoccupied shift register bits.

An optical link is used to provide the control signals to the SCA and calibration circuitry from the off-chamber electronics. An HP-1024 has been selected for this application. This approach removes the burden of having a radiation hardened SCA controller on-chamber.

VII. Radiation Tolerance

The approach to the development of the system architecture described above is primarily a function of the radiation conditions imposed on the CSC chambers. The worst case radiation conditions are:

ionizing dose of 4.4 krad/yr and neutron flux of $7 \cdot 10^{12} \, n/cm^2/yr$. Development of the system architecture centered on single event effects (SEU's) of CMOS logic elements. The design approach adapted to minimize this problem was to remove as much digital hardware from the chamber as possible, specifically the SCA controller. The trade-off is that an optical receiver is required on-chamber to receive control information. A test set is presently being developed to characterize the optical PIN diode and de-serializer when irradiated. Tests are expected to be completed by 2001.

Multiplexing of ADC data to the G-Link transmitters will be performed by COTS shift registers. This decision was based on the NRE cost to develop a rad-hard ASIC for this simple function. COTS qualification based on the ATLAS policy will be necessary. Other COTS items to qualify include an AD8042 op-amp, AD9042 ADC and MC10H116 ECL differential receivers. These items are common to the LAr FEB, and will be qualified with a joint effort among the two detector groups.

Ionizing radiation studies of the preamp/shaper have been completed. Four samples have been tested at BNL to 1Mrad. Results shown below indicate no significant effects from ionizing dose.
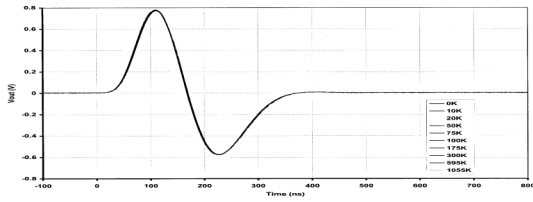
Figure 6. Pulse shape (offset subtracted)
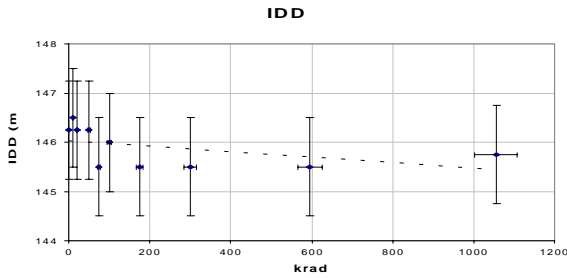
Figure 7. IDD
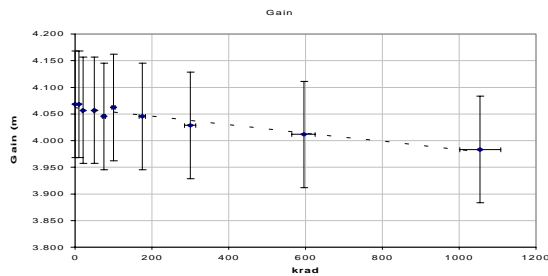
Figure 8. Gain
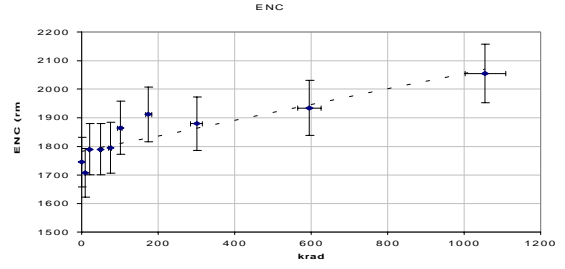
Figure 9. ENC
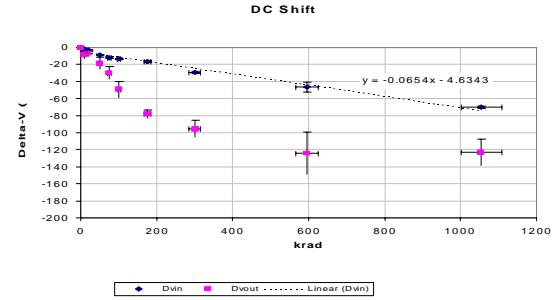
Figure. 10 DC Shift
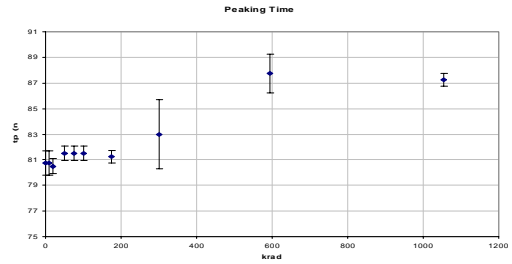
Figure 11. Peaking Time

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A Radiation Study of Analog-to-Digital Converters for a Particle Physics Detector at the Large Hadron Collider

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Junior Paper
Adviser: Peter Denes

December 8, 1997

Benjamin Lev   2

1   The Context

1.1   Introduction

The goal of high-energy physics, also known as particle physics, is to study the most fundamental constituents of matter and the forces that govern their behavior [1]. This is the pursuit to understand the universe at its most fundamental level. Physicists study the mass, charge, spin, lifetimes, and interactions of these fundamental particles to achieve this goal [2]. $E = mc^2$ states that energy is proportional to mass: higher energies are required to create heavier particles. The tools physicists use to study these properties are primarily particle accelerators and particle detectors. Particle accelerators are large and expensive machines that accelerate particles to high energies. These high-energy particles are then made to collide with stationary or moving particles. The collision of these initial particles produces a zoo of different particles of various energies and momenta. Particle physics detectors are designed to detect these particles and measure their kinematics.

The Standard Model, a collection of theories, is currently the best description of these fundamental particles and forces. It is necessary to do experiments to confirm or deny predictions of the Standard Model in order to test the bounds of its validity, and to discover phenomena not predicted by the Standard Model. In this manner physicists fine-tune their knowledge of the fundamental aspects of the universe.

1.2   The Motivation for New Experiments

The last undiscovered particle predicted by the Standard Model is the Higgs boson. It is the spin zero particle that accounts for mass in the universe, and there may be more than one Higgs boson. The discovery of this particle is crucial to the validity of the Standard Model. Supersymmetric theory (SUSY) attempts to unify the two classes of particles in the universe, bosons and fermions[1], by introducing as-of-yet undetected supersymmetric particles. Many important theories are based upon the existence of these particles.

The two highest energy particle accelerators in the world, the TEVATRON at Fermilab in Illinois and the Large Electron-Positron Collider (LEP) at the European Laboratory for Particle Physics (CERN) in Geneva, Switzerland, so far have not found these particles. If these particles exist, then they may only be produced by higher energy accelerators. The interest in finding these particles, other particles not mentioned, and the ever present drive to search for the unknown is the motivation for building higher energy particle accelerators.

1.3   The Large Hadron Collider

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[1] Bosons have integer multiples of spin and fermions have half-integer multiples of spin.

The Large Hadron Collider (LHC) is a particle accelerator that will be built by the year 2005 at CERN. The search for the Higgs boson, for supersymmetric particles, and for the unknown are among its top priorities [3]. The LHC will accelerate protons in counter-rotating beams, and bunches of protons will collide every 25ns. Head-on collisions between the protons in the LHC will produce higher energies than LEP and the TEVATRON at a higher luminosity. The maximum beam energy for the protons in the LHC will be 7 TeV (trillion electron volts). This is seven times larger than the TEVATRON's beam energy and one-hundred times larger than LEP's beam energy [4].

Luminosity is

$$L = \frac{I \cdot N \cdot f}{4\pi \cdot \sigma_x \cdot \sigma_y},$$

where I is the intensity per bunch of particles in the beam, N is the number of bunches per beam, f is the revolution frequency of the bunches, and $\sigma_{x,y}$ are the horizontal and vertical beam sizes at the interaction point [5]. The luminosity of LHC is $1\mathrm{x}10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, and this high value means that the LHC is a high luminosity accelerator. This is two orders of magnitude larger than LEP and the TEVATRON. High luminosity is desired for the following reason: the de Broglie wavelength of a particle is $h/p \propto 1/E$, and the cross section (~effective area) of protons decrease as E^{-2} [6]. This means that for higher energies, collisions between protons are less likely. Many of the most interesting processes are very rare. Since the product of the luminosity and an interaction's cross section (whose dimension is area) is equal to the frequency of that interaction, luminosity is a measure of the frequency of occurrence of rare interactions. High luminosity is needed to ensure that rare high-energy interactions can be thoroughly studied.

Why choose a proton-proton collider such as the LHC? A circular electron-positron collider has the problem of synchrotron radiation. When a charged particle is accelerated, as it is when traveling in a circular trajectory, it emits radiation. The energy loss due to this is proportional to $(E/m)^4$, where E is the maximum beam energy and m is the mass of the accelerated particle. An accelerator of this type with energies above 300 GeV is not feasible. A linear electron-positron collider is cheaper for the opposite reason, but because of its linearity, achieving high collision rates at high energies is difficult [1]. Since the mass of a proton is ~2000 times larger than the mass of an electron, the energy loss due to synchrotron radiation from a proton is $\sim 10^{-13}$ that of an electron at the same energy. As a result, the limiting factor of a circular proton-proton collider is the cost of the magnets. Since the LHC can produce the desired energies and luminosity while staying under the cost limit of the magnets, it is the reasonable choice.

1.4   The Compact Muon Solenoid

There will be four detectors at LHC: A Toroidal LHC Apparatus (ATLAS); the Compact Muon Solenoid (CMS); A Large Ion Collider Experiment (ALICE); and LHC-B. ATLAS and CMS are general purpose detectors. ALICE will study collisions between heavy ions, and LHC-B will study CP violation in B-meson decays [7]. There are two general purpose detectors at LHC because each detector can only optimally measure a

CMS
A Compact Solenoidal Detector for LHC
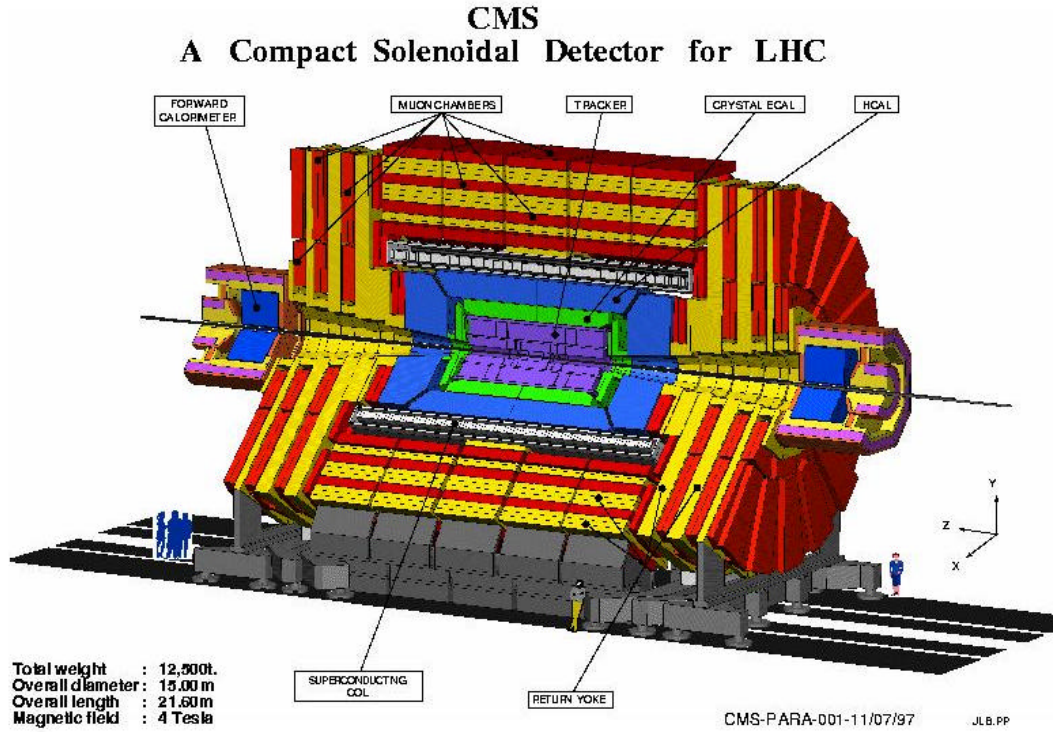
Figure 1.4.1. Three dimensional slice of CMS indicates size and positions of sub-detectors.

subset of all parameters [2], and because it is necessary to cross-check new results and discoveries. This paper will focus on CMS. Figure 1.4.1 shows a three dimensional rendering of CMS, and one can see that the detector almost completely surrounds the interaction point allowing particle detection in almost all directions.[2]

CMS is optimized to make precise measurements of "muons[3], electrons, and photons over a large energy range and at high luminosity" [8]. To accomplish this goal, the detector must be close to the beampipe carrying the protons, and have a huge magnetic field inside the detector to achieve high resolution. The trajectories of moving charged particles are bent according to

$$\mathbf{F} = q\frac{\mathbf{v}}{c} \times \mathbf{B} \ ,$$

where **F** is the force acting on the particle, q is the charge of the particle, and **B** is the magnetic field. Increasing the bend in a particle's trajectory increases the precision in the measurement of the particle's kinematics. The amount the particle's trajectory is bent is directly proportional to the **B** field and inversely proportional to its momentum. Accurate measurements of high momentum particles require the presence of a large **B** field in the detector. CMS is constructed about a solenoid with superconducting coils that will generate a homogenous 4 Tesla magnetic field.

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[2] The detector cannot intersect the beampipe and thus cannot detect particles in the beampipe.

[3] Muons are particles similar to electrons but two-hundred times more massive and exist for only 10^{-6} s.

There are five sub-detectors within CMS. The collective goal of the sub-detectors is to piece together what happened immediately after a proton-proton collision. Since the protons collide within the beampipe, an unobservable region, the sub-detectors must be extremely accurate to enable physicists to determine what happens inside the beampipe by extrapolating data into this region.

The innermost sub-detector, the tracker, is a collection of smaller detectors whose goal is to reconstruct the trajectories (momentum) of each passing particle and to be sensitive enough to allow the reconstruction of the spatial origin, the vertex, of each particle even when the vertex is in the beampipe. In general, the detector measures the location of small currents generated when an ionizing particle crosses arrays of small strips of silicon $300 \mu m$ thick. In this manner, the detector can resolve the position of a particle to within a few tens of micrometers [8].

Surrounding the tracker is the electromagnetic calorimeter (ECAL). This detector will be discussed in greater detail below. The hadron calorimeter (HCAL) surrounds the ECAL and measures the "energies and directions of particle jets," showers of particles resulting from interactions of incoming hadrons with material in the detector. HCAL also aids in measuring neutrinos[4] and muons, and is composed of alternating layers of plastic scintillator tiles and copper or stainless steel absorbers [8]. A scintillator is any material that emits light when an ionizing particle enters the object. The absorbers induce hadronic showers and the plastic scintillators measure the particle's energy and location.

The outermost sub-detector is the muon detector. The goal of the muon detector is to identify muons, trigger on events depending on muon detection characteristics, and to accurately measure the muon's momenta over a large energy range. There will be 10^9 interactions per second at LHC. Since only 10^7 interactions per second can be processed, a triggering system is required to select the interesting events [8]. The muons are detected by arrays of drift chambers. Each drift chamber contains many $50 \mu m$ diameter stainless steel wires strung inside and is filled with an $Ar\text{-}CO_2$ gas mixture. As a muon enters the chamber, it ionizes the gas and the free electrons collect on adjacent wires. A current is detected on the nearby wires, and with the knowledge of the time it takes for an electron to drift to these wires, the position of the muon is measured.

1.5   The Electromagnetic Calorimeter

The ECAL uses ~100,000 scintillating crystals, made of lead tungstate ($PbWO_4$), to measure the energy of photons, electrons, and positrons. Since one of the ways a Higgs boson can decay is to decay into two photons, the ECAL is very important to the physics that will be done at LHC. As shown in Figure 1.5.1, the crystals almost completely surround the proton-proton interaction point, enabling ECAL to detect particles in almost all directions.

Energetic photons interact with matter by pair production, the production of an electron and a positron from a photon. Through the bremsstrahlung process, electrons

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[4] Since neutrinos do not interact, HCAL "measures" them by measuring their absence. Roughly, by subtracting the total energy and momentum in an event from the sum of the detected energy and momentum, one can find the "missing" energy and momentum of the neutrinos.
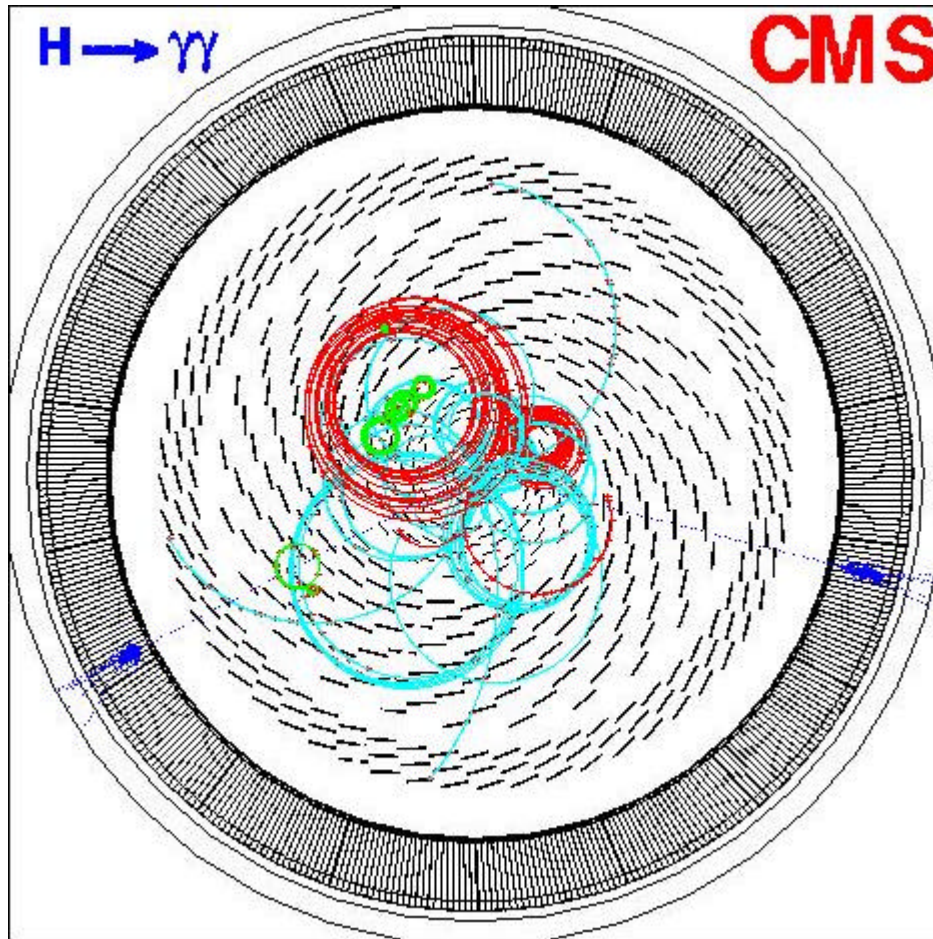
Figure 1.5.1. This is a slice of the ECAL perpendicular to the beampipe. The lead tungstate crystals are the slim rectangles pointed towards the center of the detector. Also shown is a simulated detection by ECAL of the two photons produced from the decay of a Higgs boson.

and positrons interact with matter to radiate photons. When energetic photons, electrons, and positrons enter the lead tungstate crystals, they undergo the above two processes until the resulting photons, electrons, and positrons are of energies comparable to electrons in the crystal lattice. This is called an electromagnetic shower. The lattice electrons are excited out of their ground state and upon relaxation emit photons in a narrow frequency range. These low energy photons are detected by an avalanche photodiode (APD) attached to the end of each crystal. The APD generates a current proportional to the number of incident photons which is proportional to the energy deposited in the crystal by the incident particle. The lead tungstate crystals are made long enough so that all of the energy of an incident photon, electron, or positron is deposited in the crystal. This current, which is proportional to the total energy of the detected particle, is processed by a series of electronics called the readout chain to produce two signals which are sent out of the detector by way of fiber optic links. One of the signals is sent to the trigger[5] to help decide if an event is worth saving, and the other signal is the value of energy deposited in a specific crystal in an event. More specifically, the readout chain consists of electronics to

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[5] The trigger system decides which events are rare high-energy events.

convert the APD current to a signal, an ADC to digitize this signal, and interface electronics to send the signal to the trigger and data acquisition systems [8].

The design of the readout electronics is subject to several severe constraints. Its components must fit into the compact space dictated by the overall CMS detector design [9]. The protons in the LHC collide every 25ns, and as a result the electronics must operate at 40 MHz. Since an individual crystal must measure energies up to 2 TeV, the dynamic rage of the electronics must be at least 16 bits [9]. The extremely high radiation environment of the detector requires the electronics to be resilient to these radiation levels. This latter constraint is the subject of the rest of the paper.

2   A Radiation Study of ADC's

2.1   The Radiation Environment

The high luminosity and high beam energy of the LHC will create an exceptionally harsh radiation environment for CMS [10]. This severe radiation environment can impair or disable crucial components in the detector, and a detector not specifically designed to function in this environment will be useless. As a result, the radiation environment is a large concern for the designers of CMS, and many projects are currently underway to insure every component's resistance to radiation damage.

Most of the radiation damage in CMS is caused by low energy (<1 GeV) particles. Protons have a high cross section[6] for interacting with themselves, and there are many secondary particles produced in proton-proton collisions that enter the detector. Since these particles have a typical energy of 300 MeV, they are very dangerous to material in the detector. Although other hadronic particle accelerators have a similar problem, the high luminosity and high beam energy of LHC makes this problem uniquely acute [11]. The high luminosity of LHC introduces a large flux of particles in the detector, and the high beam energy of LHC causes large showers of low energy particles [10]. This high background level of particles influences ECAL measurements by masking the detection of interesting particles. The entrance of two or more particles into one crystal makes it difficult to distinguish their identity. Decreasing the granularity of the detector, using ~100,000 crystals, helps to reduce this problem.

There are two types of particles that cause damage in CMS: particles that ionize material, and particles that interact with nuclei in material [12]. Ionizing radiation deposits energy in a material by stripping bound electrons from nuclei. Charged particles such as electrons, photons, and protons are capable of this, as are neutral pions[7] which decay into two photons. Particles that interact through the strong force, such as protons and neutrons, can interact with nuclei in a material. This causes damage to a material when the interaction changes the composition of the nuclei, thereby changing the properties of the material.

These two components of the radiation field cause different amounts of damage to different material [10]. It is necessary, therefore, to speak of the two sources of radiation damage separately. The rad[8], radiation absorbed dose, is the energy deposited in an object, and is the quantity corresponding to ionizing radiation. One rad is equal to 10 J/kg or equivalently, 6.24×10^{10} MeV/kg. The measure of the component of the radiation field that causes damage by nuclear interactions is the flux of particles through a material. Flux is the number of particles passing in a unit time through a unit area normal to the beam of particles. Fluence is the time integral of flux. The energy of neutrons at the LHC peaks at about 1 MeV. Because neutrons of this energy are the most damaging particle to nuclei, flux in this context is expressed in terms of the number of neutrons per cm^2 per second.

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[6] The cross section is the probability of interaction between two particles. Since classically it can be seen as the effective area of the target particle, the cross section is measured in units of area.

[7] Pions are hadronic bosons with a mean life of 2.6×10^{-8} s.

[8] The equivalent SI unit of absorbed dose is the Gray (Gy), which is equal to one joule per kilogram.

Ionizing radiation damages electronics by the deposition of charge inside semi-conductors, and neutron flux damages the semi-conductor lattice. For example, excess charge can prevent transistors from turning off [11]. The ECAL readout electronics will receive a 1 Mrad dose and a fluence of $2x10^{13}$ n/cm^2 [9]. Since a significant amount of radioactivity from activated[9] material in the detector will linger for a long period of time after the beam is turned off, the electrical components will not be able to be replaced. Consequently, the readout electronics must perform within tolerances for the entire ten year operation of CMS, and to insure this, each type of electrical component must be tested for its susceptibility to radiation damage. The remainder of this paper will discuss the radiation test of the ADC's.

2.2   The Study

During the summer of 1997, Benjamin Lev, under the supervision of Peter Denes, conducted a study of the effects of radiation on analog-to-digital converters (ADC's) that will be in the ECAL of CMS. An ADC converts a continuous voltage, an analog signal, to a series of discrete voltages, a digital signal. Logical operations are easier, faster, and more accurate to perform on digital signals, and this is why the ADC is of great importance to ECAL front-end electronics.

The simplest model of an ADC is the Wilkinson ADC.
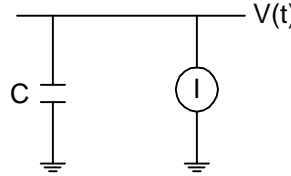
Figure 2.2.1. The circuit layout for a Wilkinson ADC.

In the above circuit, $V(t = 0)$ is the signal to be digitized, the circuit component associated with I is a constant current source, C is the capacitance of the capacitor, and $V(t)$ is the measured output voltage.

$$V(t) = \frac{Q(t)}{C} \quad , \quad \frac{dV(t)}{dt} = \frac{-I}{C}$$

Since I and C are constants, the slope of $V(t)$ is constant. The time derivative of $V(t)$ is found from the known constants I and C. By measuring the number of ticks the clock has counted when $V(t)$ reaches zero, one can find $V(t = 0)$ from $Q(t = 0)$ in terms of ticks. Once calibrated, these ticks represent a quantized voltage, and the signal has been digitized. Modern ADC's are smaller and faster[10]. An N-bit ADC can digitize an analog signal by assigning the signal one of 2^N equal quanta known as channels. The number of channels assigned corresponds to the amplitude of the analog signal. The conversion

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[9] A material is activated when incident radiation causes the material itself to emit radiation.

[10] The Analog Devices Data Converter Reference Manual Vol. II provides a good discussion of modern architectures [13].

becomes more accurate with increasing N since the discrete spectrum of channels more closely approximates a continuous spectrum.

The ADC being evaluated for use in the ECAL of CMS is the AD9042 , a 12-bit converter made by Analog Devices, Inc. (ADI). Operating at 40 MHz, this 12-bit converter assigns an input signal to one of 4096 channels corresponding to a range of zero to one volt. The ECAL will have ~100,000 ADC's corresponding to one ADC per lead tungstate crystal. ADC chips are made on wafers of silicon with 32 chips per wafer. One cannot do radiation tests on all 100,000 ADC's from all 3,407 wafers. Besides taking too much time and resources, this would make all the chips unusable. If, instead, a small fraction of the chips on a wafer represent the quality of all the chips on the wafer, then the number of chips requiring testing is dramatically decreased. The goal of the study is to determine the radiation sensitivity of these chips, and to show that a sample of chips can represent the quality of all the chips on a wafer.

Each chip was tested for initial performance, irradiated, and tested in the same manner for final performance. Thirty of the 32 chips from each of the 16 wafers for a total of 480 chips were tested. The testing method is based on a frequency domain technique which is standard in industry (Harjani, 2101). Using a Hewlett Packard (HP) 3335A Synthesizer/Level Generator, sine waves are sent through the ADC and the digitized signal is captured by a data acquisition board (DAQ) in a PC. A program written in Visual Basic (VB) talks to the HP through a GPIB cable, controls the procedure, and takes data. Eight combinations of sine frequencies and amplitudes are used for each ADC. The frequencies are 1.2 MHz, 2.5 MHz, 5 MHz, and 9.6 MHz, with each at amplitudes of 2.5 dBm and -23.5 dBm. A dBm is a commonly used unit of voltage in electrical engineering:

$$\text{y dBm} = 20 \log\left(\frac{\text{x Volts}}{.233607 \text{ Volts}}\right); \ 2.5 \text{ dBm} = .4217 \ V_{rms}; \ -23.5 \text{ dBm} = .0211 \, V_{rms}.$$

The sampling frequency of the ADC is 40 MHz, which corresponds to the proton-proton collision frequency in the LHC, and consequently, the frequency of incoming data. The choice of the set of frequencies, 1.2 MHz, 2.5 MHz, 5 MHz, and 9.6 MHz, was made so that the sampling frequency is an integer multiple of two frequencies and not an integer multiple of the other two. The Fourier transform of the non-integer multiple data sets has a spectral leakage effect added to the signal transform. This effect is discussed later. Using both integer and non-integer input frequencies tests the only two possible types of input frequencies.

The VB data taking program records 4096 data points for each frequency-amplitude combination and saves the data sets to a file. The data for each combination is sent through a fast Fourier transform (FFT) routine. This is done in real time to check the performance of the test set-up and to get a qualitative description of the raw data (the unFFT'd data) since problems are visually obvious when viewed in the frequency domain. The chip is seated in a special socket that allows quick and easy chip exchange. The socket is connected to a board that plugs into a CAMAC, which is connected to the PC and the HP. The information from the chips are read out by devices called FIFO's, First-In First-Out. These devices store and order incoming data, giving the logic of buffering events. Two 8-bit FIFO's read out the ADC. One reads the lower 8-bit and the other the upper 4-bits. On occasion a glitch with the clocks causes FIFOs to become out of step,

and this results in a bit mismatch wherein two or more data points are added or subtracted together. It is easy to see when this occurs by looking at a plot of the raw data. The VB data-taking program includes a routine that manually shifts the first 8-bits and the last 4-bits with respect to each other, takes the Fourier transforms of the shifted sets, compares the transforms, and selects the cleanest transform, thereby selecting the data set without bit mismatch. All this is done during data-taking. The VB data-taking program also assigns a unique number to each chip and the eight data sets for each chip. These identification numbers consist of the wafer number, the tray number (the physical tray where all the chips of a wafer are placed), and set of two numbers identifying the position of a chip within a wafer. These numbers are significant for traceability if a chip malfunctions or is destroyed by the radiation. One would want to know why that specific chip was destroyed, and with traceabilty, ADI can try to determine if the chip was manufactured differently.

The experiment was conducted over a period of a week at the Paul Scherrer Institute, which is the Swiss National Laboratory in Villigen, Switzerland. The ADC's were bombarded with 64 MeV protons from the OPTIS proton/pion beam. Each ADC was tested with each frequency-amplitude combination, placed at the end of the beam pipe, irradiated, and re-tested using the same test set-up. The amount of time each ADC needed to be irradiated by the OPTIS beam to simulate the 1 Mrad dose and the fluence of 2×10^{13} n/cm^2 that the ADC's will receive in CMS is calculated as follows:

The ADC chip can be approximated as a silicon crystal. The mean rate of energy loss in silicon by a minimum ionizing particle (MIP) is ~1.66 MeV cm^2/g [4]. This can be found from the Bethe-Bloch equation,

$$-\frac{dE}{dx} = \frac{4\pi n z^2 e^4}{m_e v^2}\left[\ln\frac{2m_e v^2}{I\left[1-(v/c)^2\right]} - \left(\frac{v}{c}\right)^2\right],$$

where ze is the charge of the incoming particle, v is the velocity of the incoming particle, n is the number density of electrons in the target material, and I is the mean excitation potential of the atoms in the target material. The density of silicon is 2.33 g/cm^3, and the surface area and the thickness of the chip are about .25 cm^2 and 1cm, respectively. The mass of the chip is $(.00233 \text{ kg/cm}^3)(.25 \text{ cm}^2)(.1\text{cm}) = 5.8 \times 10^{-5}$ kg.

$$\Delta E = (1.66 \text{ MeV cm}^2/\text{g})(2.33 \text{ g/cm}^3)(.1 \text{ cm}) = .39 \text{ MeV/MIP}$$

The radiation absorbed dose per minimum ionizing particle is

$$\frac{(.39 \text{ MeV/proton})}{(5.8 \times 10^{-5}\text{kg})(6.24 \times 10^{10}\text{ MeV/kg})} = 1.1 \times 10^{-7}\text{rad/MIP}.$$

One proton deposits roughly 5 times as much energy in a material as does a minimum ionizing particle. This was measured by Peter Denes at the Pi-M1 beam of protons and pions at the Paul Scherrer Institute. The protons have an energy of about 62 MeV, which is very similar to that of OPTIS, and at this energy pions are minimum ionizing particles. The ratio of dE/dx of the protons to the dE/dx of the pions resulted in a factor of 5. This was confirmed by a simulation run on the program GEANT, which simulates how particles

interact with detectors. The radiation absorbed dose per proton is 5.5×10^{-7} rad/proton. The proton flux at OPTIS is 1×10^{9} protons/(second cm^2). The ADC's receive a dose of 1 Mrad in

$$\frac{1 \text{ Mrad}}{[1 \times 10^{9} \text{ protons/(second cm}^2)][5.5 \times 10^{-7} \text{rad/proton}][.25 \text{ cm}^2]} = 7272 \text{ seconds} \cong 2 \text{ hours.}$$

The fluence of protons in two hours is 4.5×10^{12} p/cm^2, and the corresponding neutron fluence is 9×10^{12} n/cm^2, since a 62 MeV proton does as much damage as two 1 MeV neutrons [14].

Along with the aforementioned approximations, the flux of protons at OPTIS is not perfectly stable, and consequently, the two hour calculation is only a rough estimate. 416 chips were irradiated for two hours, 32 for four hours, and 32 for eight hours. Because the calculation is linear in time, the four hour irradiation corresponds to a 2 Mrad dose and 1.3×10^{13} n/cm^2, and the eight hour to a 4 Mrad dose and 3.6×10^{13} n/cm^2. Chips were irradiated longer than two hours in an attempt to find the maximum dose before the onset of obvious radiation damage.

2.3   Analysis

As mentioned earlier, the frequency-domain based testing is the standard technique for the analysis of the performance of an ADC. This involves digitizing a pure sine wave, taking its Fourier transform, and using this transform to extract parameters that characterize the ADC's performance. This is the general format that the analysis technique is based upon. The analysis technique is qualitatively described below, followed by a proof of its validity.

A sine wave input is used, as opposed to a DC input, to be able to study the ADC's ability to digitize signals that vary in time. A sine wave is also the easiest non-DC waveform to analyze, since its Fourier transform is a delta function at the frequency of the sine wave. Each ADC has associated with it sixteen data sets: eight sets for the eight frequency-amplitude input sine wave combinations taken before irradiation; and eight similar sets taken after irradiation. Each data set is the digitized input sine wave, but is not purely sinusoidal. Various errors in the testing and digitizing process distort the pure input sine wave. This raw data waveform is fit, using a least squares fitting routine, to a pure sine wave, thereby finding the signal amplitude and DC offset of the pure sine wave component of the signal. This fitted sine wave is then subtracted from the data, creating an error data set. Since this input sine wave is a pure sine wave, all aspects of the original sine wave are contained in the fitted sine wave, and what remains after the difference of the data and the fitted sine wave are the errors. The error power spectrum, the amount of error per frequency, is found from the fast Fourier transform of the error data set. The signal to noise ratio (SNR) is found by dividing the signal amplitude by the root mean squared (rms) amplitude of the error spectrum. The SNR, expressed in decibels, is a simple, commonly used indicator of an ADC's performance. Another similar parameter is the spurious-free dynamic range (SFDR), expressed in decibels. This is the difference between signal amplitude and the largest spectral component, excluding the signal peak. A decrease in SFDR indicates a decrease in ADC performance since non-signal spectral

components are increasing in amplitude. These four parameters, gain, offset, SNR, and SFDR, are found for each frequency-amplitude combination in both the irradiated and non-irradiated data sets. Finally, the change in an ADC's performance is given by the difference between the irradiated data sets' four parameters and the non-irradiated data sets' four parameters.

2.4   Proof of Technique

It is not immediately clear that this technique actually does produce the gain, offset, SNR, and SFDR. A proof of validity of technique is required. The data can be represented in the form $f(t) = A\sin(\omega t_i) + \mu + g(t)$, where t denotes the discrete time variable, and the sine term is the pure sine wave component of the data. The μ term is the offset, and $g(t_i)$ is the error function. The error function encompasses all the errors that add to the sine term to make it imperfect. $g(t)$ is determined by the following: the input signal, $s(t)$, is a pure sine wave to the accuracy of the HP sine generator and is represented as $s(t) = A\sin(\omega t) + \mu$. The error function is $g(t) = f(t) - s(t)$. One determines $s(t)$ by doing a least squares fit of $f(t)$ to the model function $y(t; A', \mu') = A'\sin(\omega t) + \mu'$, where A' and μ' are the fitting parameters. If this fit were performed on $s(t)$ it is clear that $A' = A$ and $\mu' = \mu$ would give the best fits, but in the technique the fit is performed on $s(t) + g(t)$. For the technique to be valid this fit must still produce $A' = A$ and $\mu' = \mu$ regardless of the added $g(t)$ term.

Assigning $T = A\sin(\omega t_i) + \mu - A'\sin(\omega t_i) - \mu'$,

$$\chi^2 = \sum_{i=1}^{N}\left(\frac{T^2 + 2Tg(t_i) + g^2(t_i)}{\sigma_i^2}\right).$$

To minimize χ^2, one must take the partial derivatives of χ^2 with respect to A' and μ' and set each equation equal to zero.

$$0 = \frac{\partial\chi^2}{\partial A'} = \frac{\partial}{\partial A'}\sum_{i=1}^{N}\left(\frac{T^2 + 2Tg(t_i) + g^2(t_i)}{\sigma_i^2}\right)$$

$$0 = \frac{\partial\chi^2}{\partial\mu'} = \frac{\partial}{\partial\mu'}\sum_{i=1}^{N}\left(\frac{T^2 + 2Tg(t_i) + g^2(t_i)}{\sigma_i^2}\right)$$

$$\frac{\partial}{\partial A'}(T^2 + 2Tg(t_i) + g^2(t_i)) = -2T(\sin(\omega t_i)) - 2\sin(\omega t_i)g(t_i) = -2\sin(\omega t_i)(T - g(t_i))$$

$$\frac{\partial}{\partial\mu'}(T^2 + 2Tg(t_i) + g^2(t_i)) = -2T - 2g(t_i) = -2(T - g(t_i))$$

The error function is small since the raw data is unquestionably sinusoidal, and the assumption $A \gg g(t_i)$ can be made. Thus

$$(T - g(t_i)) = (A\sin(\omega t_i) + \mu - A'\sin(\omega t_i) - \mu' - g(t_i)) \approx (A\sin(\omega t_i) + \mu - A'\sin(\omega t_i) - \mu') = T.$$

$$\Rightarrow \frac{\tilde{\partial}}{\partial A'}(T^2 + 2Tg(t_i) + g^2(t_i)) \cong \frac{\tilde{\partial}}{\partial A'}(T^2) = -2\sin(\omega t_i)T$$

$$\Rightarrow \frac{\tilde{\partial}}{\partial \mu'}(T^2 + 2Tg(t_i) + g^2(t_i)) \cong \frac{\tilde{\partial}}{\partial \mu'}(T^2) = -2T$$

$$0 = \frac{\partial \chi^2}{\partial A} \cong \frac{\tilde{\partial}}{\partial A'}\sum_{i=1}^{\Lambda}\left(\frac{T^2}{\sigma_i^2}\right) \text{and } 0 = \frac{\partial \chi^2}{\partial \mu} \cong \frac{\partial}{\partial \mu'}\sum_{=1}^{\Lambda}\left(\frac{T^2}{\sigma_i^2}\right)$$

These are the same two equations we would get if we had performed a least squares fit on $s(t)$ alone. This means that the least squares fit of $f(t)$ to $y(t; A', \mu') = A'\sin(\omega t) + \mu'$, will still produce $A' = A$ and $\mu' = \mu$. This means that the technique does indeed find $s(t)$, and from $g(t) = f(t) - s(t)$, finds $g(t)$. This is what is needed for this part of the technique to be valid.

$$\text{SNR} = \frac{A}{\text{rms}[G(f)]}$$

The question to be answered is whether this is really the SNR. Normally, one finds both the signal and the error spectrum from the same FFT. In this case, the SNR is found by piecing together the ingredients for the SNR. To prove the validity of this, one must prove that finding the signal amplitude and the rms error amplitude separately and then adding them together is the same as finding the signal and error amplitude from the same power spectrum. To do this one must demonstrate the linearity of the discrete Fourier transform.

The discrete Fourier transform of $f(t) = s(t) + g(t)$ is

$$\sum_{k=0}^{N-1} f_k e^{2\pi ikn/N} + R_0 = \sum_{k=0}^{N-1} s_k e^{2\pi ikn/N} + R_1 + \sum_{k=0}^{N-1} g_k e^{2\pi ikn/N} + R_2$$

$$\Rightarrow \sum_{k=0}^{N-1} f_k e^{2\pi ikn/N} = \sum_{k=0}^{N-1} s_k e^{2\pi ikn/N} + \sum_{k=0}^{N-1} g_k e^{2\pi ikn/N} + R_1 + R_2 - R_0$$

Where R is the remainder term in the discrete approximation to the Fourier transform integral, N is the number of points sampled, and the n's are the indices of $F(f_n), S(f_n),$ and $G(f_n)$. Because the remainder of the discrete approximation of the Fourier transform integral is neglected for reasonably large N, $[R_1 + R_2 - R_0] \to 0$. Thus,

$$\sum_{k=0}^{N-1} f_k e^{2\pi ikn/N} = \sum_{k=0}^{N-1} s_k e^{2\pi ikn/N} + \sum_{k=0}^{N-1} g_k e^{2\pi ikn/N}.$$

Given the above approximations, the discrete Fourier transform is linear. The different terms of a function can be separately FFT'd and then added together to equal the FFT of the original function. The signal and error spectrum can be found separately, and this technique for finding the gain, offset, SNR, and SFDR is valid.

2.5   Discussion of Technique

Why is it that the gain, SNR, and SFDR are not simply extracted from the Fourier transform of $f(t)$? This is because errors made it impossible to completely distinguish the signal amplitude from the error spectrum in $F(f)$. There are four main sources of error that contribute to $F(f)$. A discrete Fourier transform of a function will cause frequencies to "leak" into other frequencies resulting in an overlap of the original frequencies. This spectral leakage makes it impossible to completely reproduce the true frequency spectrum. Spectral leakage is the manifestation of the discreteness of the Fourier transform. The Fourier transform represents a function as a sum of sines and cosines in the frequency domain. A function is in the frequency domain when its independent variable is frequency rather than time. A discrete Fourier transform represents a function as a sum of sines and cosines whose frequencies are integer divisors of the sampling frequency. For example, at 40 MHz, unlike the discrete Fourier transforms of 1.2 MHz and 9.6 MHz sine waves, the transforms of 2.5 MHz and 5 MHz sine waves will not have spectral leakage. However, in the 5 MHz and 2.5 MHz tests, a small amount of spectral leakage is still present due to timing imperfections of the HP and ADC which cause slight variances in frequency. Although the technique of data windowing can decrease the spectral leakage effect, it cannot be completely eliminated.

The remaining errors are due to noise. For a given input frequency, the baseline of the frequency spectrum furthest from the input signal's frequency contains the least amount of spectral leakage from the signal. The amplitude of this noise baseline is larger for the 2.5 dBm input signals than for the -23.5 dBm input signals. This implies that there is an amplitude dependent noise component, and this is probably caused by error from the HP sine generator. White noise, a frequency spectrum of constant amplitude, is introduced by the test set-up, the testing environment, the CAMAC, and the cables. Finally there is noise from the ADC, which is what needs to be measured. The inability to separate the spectral leakage from the various noise contributions precludes isolating the signal, and the aforementioned technique must be used.

2.6   Results

The change in four parameters due to irradiation was measured with the goal of determining whether ADI's AD9042 ADC is suitable for use in the high radiation environment of CMS. The SNR of the ADC's did not change in the dose range that will be experienced in CMS. Neither the 2 hour irradiation period (~1 Mrad dose and 9×10^{12} n/cm^2 fluence) nor the 4 hour irradiation period (~2 Mrad dose and 1.3×10^{13} n/cm^2 fluence) induced a change in the SNR. However, the 8 hour irradiation period (~4 Mrad dose and 3.6×10^{13} n/cm^2 fluence) did induce a slight change. Figure 2.6.1 shows the SNR before and after for each chip in dBFS (decibels related to the converter's full scale). Since the SNR plots for the different input frequency tests are extremely similar, only the 9.6 MHz input signal test is shown.

Small Signal (-23.5 dBm) SNR Before ○ and After ● Irradiation
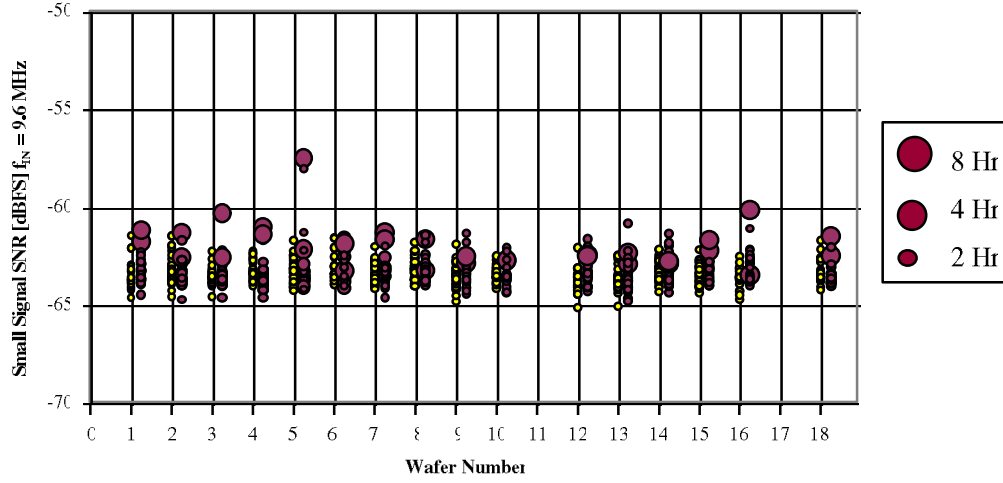
Figure 2.6.1. No change in SNR.

The SFDR also did not change for the chips irradiated for 2 and 4 hours, and did change for those irradiated for 8 hours. This is shown in Figure 2.6.2 for the 9.6 MHz input signal test.

Small Signal (-23.5 dBm) SFDR Before○ and After● Irradiation
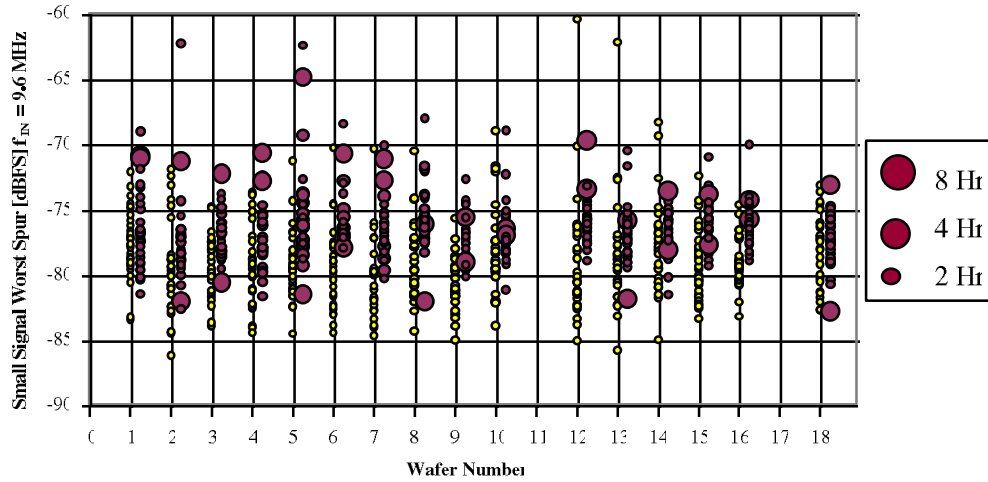
Figure 2.6.2. No change in SFDR.

The gain change is $-2.6 \pm 0.6\%$. Others have also observed slight gain changes. Figure 2.6.3 is for all chips and all input frequencies.
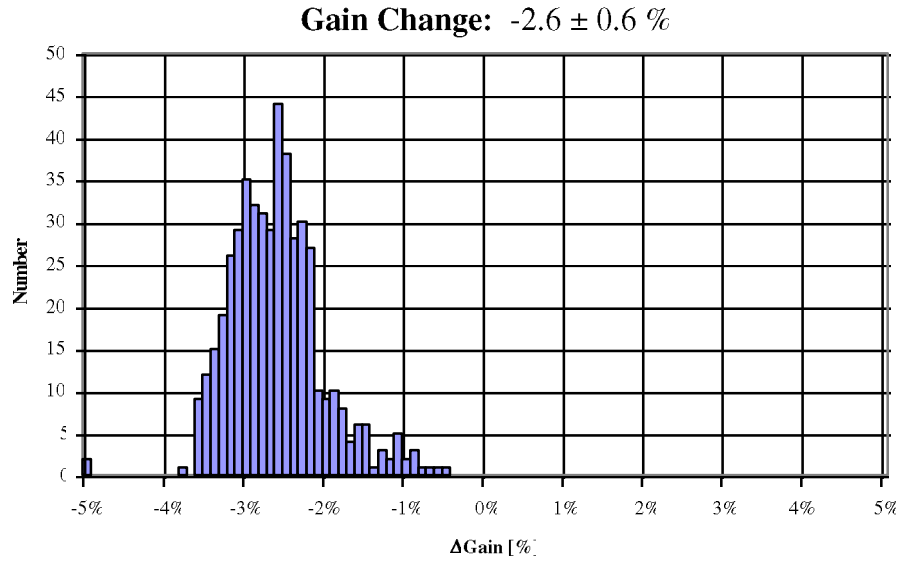
Gain Change: -2.6 ± 0.6 %

Figure 2.6.3. ADC running at 40 MHz. Input 1.2, 2.4, 5.0, 9.6 MHz.

Interestingly, the percentage gain change is inversely proportional to radiation dose, as shown in Figure 2.6.4.

Radiation Induced Gain Change
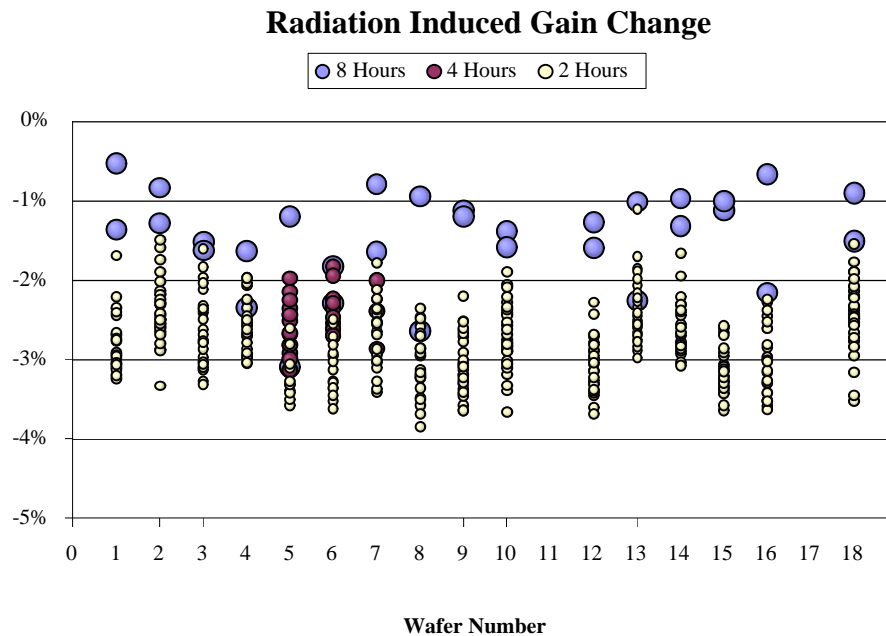
Figure 2.6.4. Inverse relationship between gain change and radiation dose.

Others have also reported an inverse relationship between gain change and total dose.

The offset change is -2.6 ± 1.7 channels $(\sim 600 \mu \text{Volts})$, but Figure 2.6.5 shows that the gain and the offset do not seem to be correlated.

Offset Change vs. Gain Change

Figure 2.6.5. Gain/Offset change not correlated

2.7   Conclusion

The results indicate that ADI's AD49042 ADC is suitable for use in the ECAL of the proposed LHC's CMS detector. Neither the SNR nor the SFDR of the ADC's are affected up to a 2 Mrad dose and a fluence of $1.3x10^{13}$ n/cm^2. Since the ADC's will only receive a 1 Mrad dose and a fluence of $9x10^{12}$ n/cm^2 during the ten year lifetime of CMS, this is more than acceptable. The offset of the digitized sine wave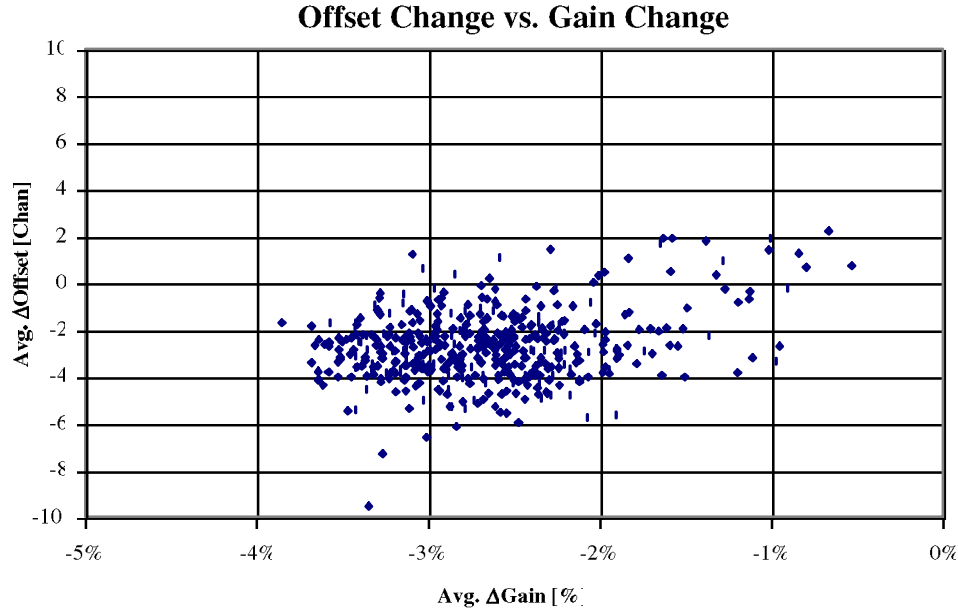s are slightly affected by the radiation dose, but for use in the front-end electronics of the ECAL, this change is insignificant for this application. The gain change is the only significant radiation-induced effect. It is possible that the proton beam dopes the silicon causing changes in the chip's resistors. This is only speculation, and further investigation is required to understand the true nature of this effect.

Because the gain change is not large and because the radiation dose will be delivered over ten years, this change in gain does not pose a problem. Since the energy response of the ECAL must be frequently recalibrated regardless of this effect, the gain change will be detected and taken into account in calibration corrections. However, this can only be done if the gain change is slow in time and all the ADC's change similarly. The Gaussian nature of the gain changes shown in Figure 2.6.3 implies that the latter condition is likely to be satisfied. This inverse gain change dependence on dose is slightly worrisome for the reason that there must be a global maximum in the gain change since the gain change is initially zero. This poses no problem if the maximum occurs near or after 1 Mrad and $9x10^{12}$ n/cm^2. If the maximum is near 1 Mrad and $9x10^{12}$ n/cm^2, then the gain change would be similar in magnitude to that measured at 1 Mrad and $9x10^{12}$ n/cm^2, and it does not matter if the maximum occurs at greater than 1 Mrad and $9x10^{12}$ n/cm^2 since the ADC will only receive 1 Mrad and $9x10^{12}$ n/cm^2. However, if the maximum occurs at significantly less than 1 Mrad and $9x10^{12}$ n/cm^2, then one cannot be sure that at a

certain point in the detector's lifetime the ADC's' gain change will not spike to unusable levels. We can be confident that this is unlikely to happen since others have found that a .5 Mrad dose induces a gain change less than that found here for a 1 Mrad dose and a and $9x10^{12}$ n/cm^2 fluence. Though unnecessary, radiation tests at lower radiation doses could be made in order to be completely confident of the viability of these ADC's.

Since none of the chips were damaged to unacceptable levels, the study shows that a radiation test on a small sample of the chips from a wafer represents the quality of all the chips on that wafer. These ADC's can be used in the ECAL, and the quality of the 109,008 ADC's can be determined efficiently. These ADC's can also be used in other fields, such as space applications, where radiation levels are near this magnitude. The year 2005 will see AD9042 ADC's taking data from LHC's CMS particle detector.

3.1   References

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Radiation Tests of MC10H116 Chips

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Abstract

We report the results of radiation tests of MC10H116 triple line receivers, which we performed to evaluate the suitability of this COTs device for use on the Front End Boards of the ATLAS LAr readout. Samples have been exposed to high intensity proton beams in order to simultaneously evaluate their tolerance to ionizing radiation, hadrons, and possible single event effects (SEE). No SEE-induced effects were observed, and the devices were shown to be sufficiently radiation tolerant to be suitable for our application.

1 Introduction

Radiation hardening the design of the ATLAS LAr Front End Boards (FEB) [1] has required the development of several custom ASICs using radiation-hard processes (both DMILL and DSM). However, for certain functions, we plan to employ commercial off-the-shelf (COTs) components. In this paper, we present the results of our radiation tests of the commercial MC10H116 triple line receiver.

2 Radiation Tolerance Requirements

Simulations of the ATLAS detector have been performed to estimate the radiation levels to which the electronics will be exposed over 10 years of LHC operation. Separate levels are provided for Total Ionizing Dose (TID in kRad), neutron-induced damage (NIEL, in 1 MeV equivalent neutrons/cm^2), and for single event effects (SEE, calculated for the total fluence of hadrons of momentum greater than 20 MeV).

The FEBs will be installed in the ATLAS detector in crates mounted directly on the signal feedthroughs of the barrel and endcap cryostats. The expected radiation levels [2] to which the FEBs will be exposed in the EM barrel are summarized in Table 1. Since the expected levels in the endcaps are approximately ten times lower than in the barrel, the qualification procedure concentrates on the case of the EM barrel.

The ATLAS radiation qualification criteria require irradiation of electronics to the expected levels multiplied by the product of "safety factors" (SF) which account for uncertainties in the simulation of the expected radiation levels (SF_{sim}), in possible low dose rate

Type of Radiation	Simulated Level
TID	5 kRad
NIEL	$1.6 \times 10^{12} \ n/cm^2$
SEE	$7.7 \times 10^{11} \ h/cm^2$

Table 1: Expected radiation levels for the FEBs mounted in the EM barrel crates, integrated for 10 years of LHC operation.

effects (SF_{ldr}), and in possible lot-to-lot variations (SF_{lot}). The safety factors to be used depend on the type of component and type of test being performed.

2.1 Safety Factors

The MC10H116 is a bipolar COTs device which, for production, we purchase from a known homogeneous lot. Table 2 summarizes the appropriate safety factors to use for both pre-selection and production tests, while Table 3 lists the resultant Radiation Tolerance Criteria (RTC).

Test	Preselection Tests				Production Tests			
Type	SF_{sim}	SF_{ldr}	SF_{lot}	Total	SF_{sim}	SF_{ldr}	SF_{lot}	Total
TID	3.5	5	2	35	3.5	5	1	17.5
NIEL	5	1	2	10	5	1	1	5
SEE	5	1	2	10	5	1	1	5

Table 2: Summary of safety factors to use in the preselection and production radiation qualification of the MC10H116, a bipolar COTs component.

Test Type	Simulated Level	Preselection RTC	Production RTC
TID	5 kRad	170 kRad	87.5 kRad
NIEL	$1.6 \times 10^{12} \ n/cm^2$	$1.6 \times 10^{13} \ n/cm^2$	$8.0 \times 10^{12} \ n/cm^2$
SEE	$7.7 \times 10^{11} \ h/cm^2$	$7.7 \times 10^{12} \ h/cm^2$	$3.8 \times 10^{12} \ h/cm^2$

Table 3: Simulated radiation levels for 10 years of LHC operation, and the Radiation Tolerance Criteria (RTC) for the MC10H116 for both pre-selection and production tests.

3 Radiation Facility

The irradiation runs were performed at the *Harvard Cyclotron Laboratory (HCL)* [3] in Cambridge, Massachusetts. The HCL, which was de-commissioned on June 2, 2002, used a proton synchrocyclotron to generate proton beams, primarily for radiation therapy. The facility could be used during the weekends for other purposes, including radiation qualification of electronics.

The HCL proton beam had a maximum energy of 158 MeV on target; irradiation at lower proton energies could be achieved by insertion in the beamline of lucite absorbers of varying thicknesses. The beam energy resolution was typically 2 - 5 MeV for energies above 100 MeV, and about 10 MeV for lower energies.

The HCL high-intensity beamline delivered a maximum flux of $\approx 3.5 \times 10^{10}$ protons/cm^2/s. The uniformity of the flux was within $\approx \pm 20\%$ over the beamspot of ≈ 1 cm diameter. The proton fluence was measured online using a calibrated ion chamber positioned in the proton beam, the signal from which was integrated and used to generated "Monitoring Pulses" (MON) after given increments of integrated proton fluence. The MON were used by the cyclotron control room to monitor the operation of the machine.

Using a 20 - 160 MeV proton beam allows us to simultaneously accumulate total ionizing dose (TID), 1 MeV-equivalent neutron fluence, and hadrons with sufficient energy to potentially cause SEE. The conversion factors are energy-dependent. For protons in this energy range, the 1 MeV-equivalent neutron fluence is somewhat higher than the actual proton fluence, though we assume a conversion factor of unity in order to be conservative. Table 4 summarizes the conversion for calculating the equivalent TID from the proton fluence.

Proton Energy (MeV)	Proton Fluence per MRad TID (10^{13} p/cm^2)
158	1.47
100	1.06
50	0.67
20	0.31

Table 4: Fluence of protons required to accumulate 1 MRad total ionizing dose, as a function of proton energy.

4   DAQ and Test Procedure

The radiation test setup utilizes the portable DAQ we developed for a variety of electronics testing and radiation qualification purposes. The DAQ is driven by a portable PC equipped with two National Instruments DAQ boards, one for digital I/O and the other for analog I/O and power connections.

A cable from the cyclotron control room provided a pulse for every MON unit. The pulses were counted using a general-purpose counter on the analog I/O board and read by the DAQ PC in order to provide online measurements of the integrated exposure.

Each DAQ I/O board is connected via its own 50-pin 75-foot twisted-pair cable to a "Sample Driver" board. The Sample Driver contains voltage regulators for providing power to the Device-Under-Test (DUT) fixture; the power supply currents and voltages can be measured through the analog I/O. In addition, four analog inputs and two DAC outputs are available to the DUT fixture. The digital I/O implements two 8-bit TTL ports, with strong TTL drivers and terminations on both ends of the cable.

For typical runs, the supply voltage and current of the DUT were monitored during the irradiation with a time resolution of 200 μs. Every second, the DAQ would record to disk the average value, RMS, maximum value and minimum value of both the voltage and current.

The DAQ was programmed to record the entire history to disk if there was a significant variation of any of the values during any one second interval.

In case of an SEL occurrence, the supply current would be expected to rise dramatically. To prevent a possible fire hazard, the DAQ was programmed to switch off the power to the DUT if its supply current exceeded a pre-set limit. To see if the device would recover from a possible occurrence of SEL, the DAQ would automatically turn the power on again after 30 seconds. After 20 such power cycles, the DAQ would turn off the power permanently, and abort the run.

5   Device Description

The MC10H116 is an ECL triple-line receiver which we plan to use for driving the SCA address and control buses. The MC10H116 is a bipolar device fabricated by ON Semiconductor [4]. The chip does not contain any internal registers or digital logic, and therefore does not present Single Event Upset (SEU) concerns. However, in addition to sufficient TID and NIEL tolerance, we must demonstrate immunity of the device to Single Event Latchup (SEL).

The pre-selection tests were performed using MC10H116FN parts packaged in a PLCC20. For the final production boards, negotiations with ON Semiconductor and a distributor culminated in an agreement wherein we ordered the full quantity of chips required from a single existing production lot. The production chips were packaged in an SOIC-16, corresponding to part number MC10H116D. Discussions with ON Semiconductor verified that the parts are identical to the MC10H116FN, apart from the package, confirming that the pre-selection tests are still valid despite the package change.

All MC10H116D production parts came from lot code 0035. As a first stage in the procurement process, we received 50 samples from this reserved lot for radiation testing. The agreement stipulated that, in the (unlikely) event that the devices did not pass our radiation-tolerance requirements, we could cancel the order without penalty. Once the radiation tests described here were successfully completed, we proceeded with the complete order and have purchased and received all of the production parts.

5.1   MC10H116 Use in Other ATLAS Applications

Various institutions have expressed interest in using MC10H116 chips in other ATLAS applications, namely in the LAr Controller Board and in the CSC readout. We have agreed to purchase sufficient MC10H116 chips from our production lot for these applications as well, and to perform the radiation qualification of the production lot such that it satisfies the requirements of all three applications.

The LAr Controller resides in the same crates as the LAr FEBs, and therefore has identical radiation tolerance criteria. However, the expected neutron level in the worst case position of the CSC readout, with a value of $RTC_{NIEL} = 2.7 \times 10^{13} \, n/cm^2$, is a factor ≈ 3.4 higher than for the LAr readout. As described later, we irradiated a subset of the production chips to these higher levels in order to satisfy this criterion.

6 Pre-Selection Tests

For the pre-selection tests, the chips were powered during irradiation and the supply voltage and current were continuously measured and recorded. However, no online AC tests were performed. Instead, the non-inverting inputs were tied to ground, and the inverting inputs were tied to V_{BB}.

A total of six samples were prepared for the first round of pre-selection tests. Five of the samples were irradiated with the final sample kept as a control. These first tests on October 15, 2000 used the lower-flux aerospace beamline at HCL, and were therefore limited in the total fluence which could be achieved. To overcome the fluence limitation, a second set of tests was performed on November 5 and 11, 2000, with the samples installed in the high intensity beamline directly in the cyclotron vault. A total of an additional 13 devices were irradiated.

Table 5 summarizes the MC10H116 chips irradiated during the two sets of pre-selection tests The 13 devices of the second set of tests were irradiated to proton fluences which exceed the LAr pre-selection RTC_{NIEL} of $1.6 \times 10^{13}\,n/cm^2$ by factors of typically 1.5 to 3 (by which point they exceed the required TID and SEE levels by very large factors).

Test Date	Number of Samples	Total Fluence ($p/cm^2/s$)	TID (kRad)
Oct. 15, 2000	3	1.1×10^{12}	75
	1	4.4×10^{12}	299
	1	8.5×10^{11}	58
	1	0	0
Nov. 5+11, 2000	8	2.5×10^{13}	1700
	5	5.0×10^{13}	3400

Table 5: Summary of pre-selection radiation tests of the MC10H116.

The voltages and currents of all samples were stable during irradiation, and there were no instances where variations during any one second interval exceeded the pre-set thresholds ($10\,mA, 100\,mV$ for $max - min$, and $5\,mA, 50\,mV$ for the RMS). The current limit of the power supply was set to $1\,A$, in order to deliver sufficient current for a real-life latchup condition. However, no occurrences of latchup were observed.

Based on these results, we consider the MC10H116 to have passed the pre-selection radiation qualification criteria.

7 Production Tests

For the production tests, we had to design a new DUT test jig due to our decision to move to the SOIC package (part number MC10H116D). The new jig was designed to allow AC measurements during irradiation, in addition to online current and voltage measurements. All three of the line receivers of the DUT could be driven with a differential clock signal, and one of three differential outputs could be observed. The input and output differential signals were transmitted over ≈ 50 m coax cables installed between the control room and the cyclotron vault.

5

During irradiation, we used an external pulse generator to send a 40 MHz differential clock signal of $\approx$ 400 mV amplitude to the MC10H116 inputs. The MC10H116 output signal was recorded using a digital oscilloscope which displayed the received signal and also measured the voltage levels and rise and fall times.

Table 6 summarizes the MC10H116 chips irradiated during the production tests. As a first step, 16 devices were irradiated on March 9/10, 2002 to proton fluences of 9.2×10^{12} n/cm^2 (15% above the LAr production RTC_{NIEL} of 8.0×10^{12} n/cm^2, by which point they exceed the reqired TID and SEE levels by very large factors). Due to the higher RTC_{NIEL} of 2.7×10^{13} n/cm^2 for the CSC readout, an additional 12 devices were irradiated on May 7 and 16, 2002 to fluences which meet or slightly exceed this level.

Test Date	Number of Samples	Total Fluence ($p/cm^2/s$)	TID (kRad)
March 9/10, 2002	16	9.2×10^{12}	626
May 7, 2002	8	2.7×10^{13}	1837
March 16, 2002	4	2.8×10^{13}	1905

Table 6: Summary of production radiation tests of the MC10H116.

No occurrences of latchup were observed. The stability of the power consumption is demonstrated by Figure 1, which displays the measured supply currents versus integrated proton fluence for the irradiated production MC10H116D samples. The devices, powered with a 5 V supply, have a typical current before irradiation of $\approx$ 82 mA. A slight change in the current with fluence is observed, amounting to less than 1 mA. This very small effect is of no consequence for operation in ATLAS. The small spikes which are seen are artifacts of the DAQ and likely result from pickup in the long cables connecting the DUT in the cyclotron vault to the external DAQ setup.

No significant variations were observed in the voltage levels or rise and fall times of the MC10H116D output signal. As an example, Figure 2 displays the pulseshape accumulated during irradiation of one production MC10H116D sample with the oscilloscope configured to infinite persistence.

8 Discussion of Results

The MC10H116D samples from the production lot passed the production NIEL and TID radiation qualification criteria for both LAr applications (FEB and Controller) and for the CSC readout.

No occurrences of latch-up were observed, during a total proton fluence (summed over the 28 production devices listed in Table 6 which were irradiated) of 4.75×10^{14} p/cm^2. The statistical sensitivity of the data, therefore, allows one to set an upper limit on the SEL cross-section of $< 4.84 \times 10^{-15}$ cm^{-2} (90% CL). Including the pre-selection samples in the total proton fluence would reduce this upper limit by a factor of about 2, but we consider only the production samples in order to have a conservative limit.

To evaluate the implications for operation in ATLAS, we must consider that each FEB uses 8 MC10H116 chips. A total of 1524 FEBs are to be installed in ATLAS. Of these, 896 FEBs, or 7168 MC10H116 chips, are used to read out the EM Barrel calorimeter, for
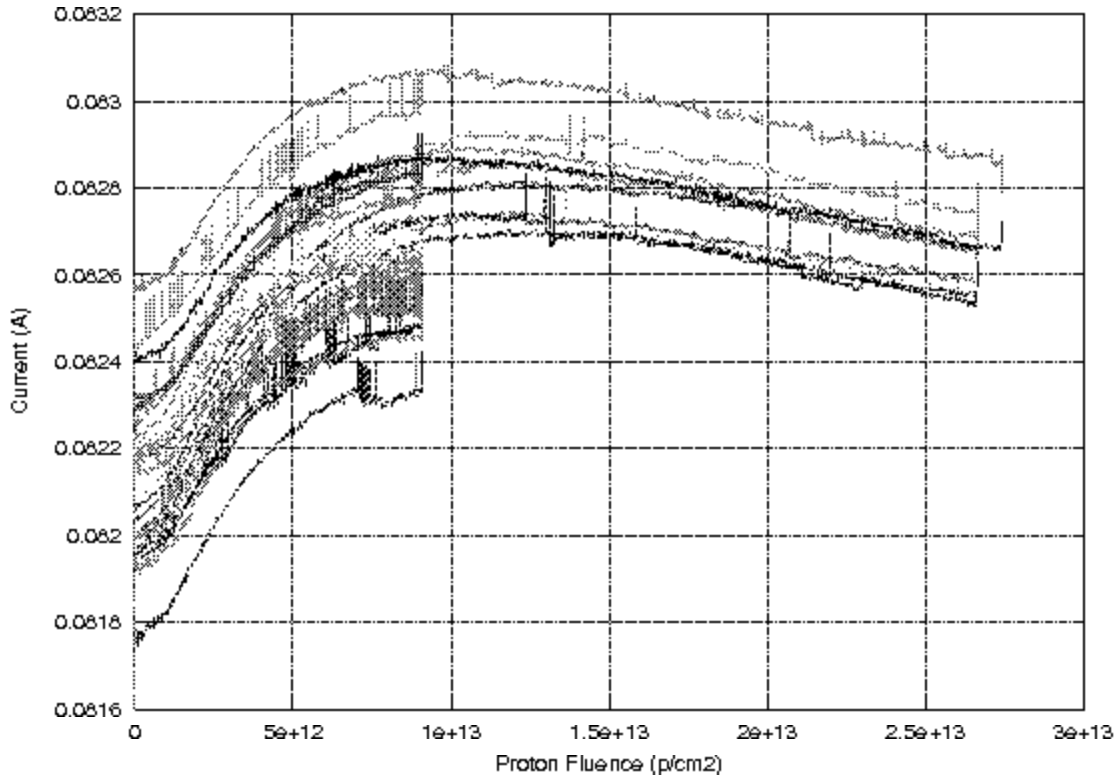
Figure 1: Measured test jig supply current versus integrated proton fluence for a number of production MC10H116D chips.

which $RTC_{SEE} = 3.8 \times 10^{12}$ h/cm^2 including the required safety factor of 5 (see Tables 2 and 3). The SEL cross-section upper limit yields, therefore, a 90% CL upper limit of about 130 SEL occurrences in the entire EM Barrel over 10 years of LHC operation (and a factor of about 10 lower in the LAr Endcaps); assuming 10^7 s of operation each year, this limit would correspond to an average of one SEL in the EM Barrel every 8.8 days of operation. While no SEL occurrences are expected, such a rate would not cause any significant operational difficulties in ATLAS. The use of current-limiting voltage regulators on the FEBs also provides added protection against fire hazards.

In conclusion, the MC10H116D devices have passed the radiation qualification process for both the LAr applications (FEB and Controller) and for the CSC readout. We have, therefore, completed the purchase of the entire set of 18200 devices needed (14600 for the LAr FEB, 2700 for the LAr Controller, and 900 for the CSC readout).

References

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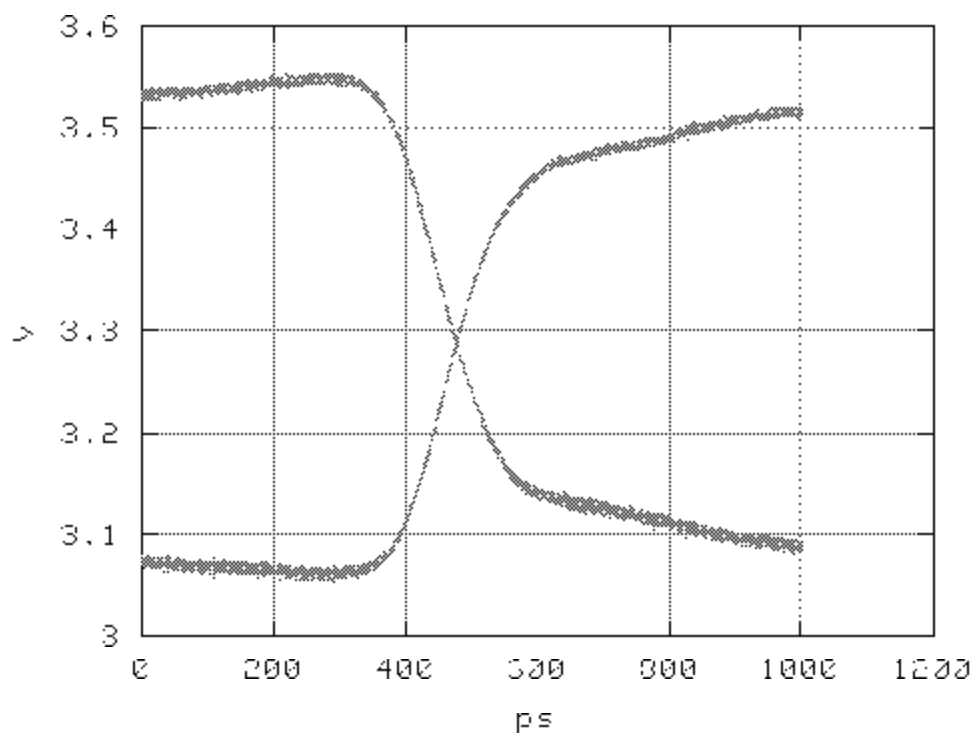Figure 2: Measured output pulse shape accumulated during irradiation of a MC10H116D production sample.

[2] These levels are based on the November 18, 2000 baseline and are available at `http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm`.

[3] For more information on the Harvard Cyclotron Laboratory, see `http://neurosurgery.mgh.harvard.edu/hcl/flyer.htm`.

[4] The datasheet for the MC10H116 can be obtained from `http://www.onsemi.com`.

Radiation Tolerance Assurance for ATLAS CSC Electronics

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1 Introduction

The ATLAS Cathode Strip Chamber (CSC) on detector electronics will be running in a highly radiating environment. The radiation mainly from neutrons and photons may inflict damage to the electronic system and jeopardize normal data acquisition or in some serious case cause fire on circuit boards. Therefore for the safety of the persons operating the experiment and the safety of the detector, it is highly desirable to have radiation tolerance assurance for all the electronic devices mounted on detector.

2 Radiation environment at the location of CSC

The radiation levels at the location of CSCs have been computed using the ATLAS Monte Carlo simulation. Assuming 180 days of ATLAS operation annually, at the worst location for radiation, the ionizing dose from photons reaches 1.1 KRad/yr (Si) and the neutron flux reaches 7.0×10^{12} neutrons/cm^2/yr which

Table 1: Neutron flux and energy spectrum at the location of Cathode Strip Chamber

Neutron Energy Range	Worst Location (KHz/cm^2)	Best Location (KHz/cm^2)
0 ~ 1 KeV	100	20
1 ~ 10 KeV	100	10
10 ~ 100 KeV	100	10
100 KeV ~ 1 MeV	100	10
1 ~ 10 MeV	20	5
10 ~ 100 MeV	10	1
100 MeV ~ 1 GeV	5	1
Total	450	50

converts to 1.8×10^{12} 1-MeV-equivalent neutrons per square centimeter per year. At the best location, the radiation levels are an order of magnitude lower. Table 1 lists the detailed neutron flux and energy spectrum at the best and worst locations for radiation of the Cathode Strip Chamber. The worst location for radiation occurs at R= 89 mm, and Z = 725 mm; and the best location is at R= 197 mm, and Z = 690 mm.

3   Radiation effects to electronic components

The damages caused by neutron and photon radiations to electronic devices can be grouped into three categories based on their damaging mechanisms:

- **Total Ionizing Dose Effects** induced by photons. Photon causes ionization (electron-hole pair production) along its track in Si or SiO_2. Because of their high mobility, electrons will drift out of the oxide layer quickly. Meanwhile the holes produced in the ionization processes have very low mobility, most of them will be trapped in the oxide. The effect is that there is net positive charge trapped in the oxide layer in silicon devices. Especially at room temperature, the trapping is long term. The positive charge accumulated in the oxide layer will cause noise increase and electric parameter drifting out of its dynamic range hence claim the death of a silicon device.

- **Displacement Damage** caused by non-ionizing energy loss of heavy particles such as neutrons or protons in materials. Neutrons or protons collide with the atoms in material inducing dislocation of atoms or amorphization of the material structure. In silicon devices, the effective majority carrier concentration decreases due to displacement damage which effectively increases the resistivity of the material. Severe displacement damage could induce type inversion of silicon for example $N \rightarrow P$, hence cause the dysfunction of a device

- **Single Event Effects** induced by single energetic heavy particles such as neutrons or protons passing through Si or SiO_2. Most of the neutrons pass through materials by elastic scattering or diffraction and inflict displacement effect, but when neutron energy is greater than an energy threshold, nuclear reactions such as n + Si $\rightarrow$ p +Al and n + Si $\rightarrow$ α + Mg start to come on to the stage to play an important role. The secondary charged ions produced in nuclear reactions will produce further ionization along its track. The charges along the track cause a transient current which, if big enough, enables digital flip-flops to change state, therefore induce data corruption. This phenomenon is called "Single Event Effects". The Single Event Effects can be categorized into three classes based on the degree of the radiation damage to the electronics devices

    1. Single Event Upset, the upset is transient; a reset or rewrite of the device will restore normal behavior thereafter.

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2. Single Hard Error, an upset causes permanent change to the operation of a device, for example, a stuck bit in memory chip.

3. Single Event Latchup/Burnout/Gate Rupture (destructive), very high current in a local area causes neighboring gates latchup or chemical bonds rupture or gates burnout.

There have been a number of studies on the soft error rates (Single Event Upset). Studies show that the SEU cross sections have the same sensitivity to neutrons and protons when the energy of the particles is higher than 20 MeV and the SEU cross section has a flat distribution with respect to the neutron energy. In ATLAS environment, the SEU errors induced by neutrons with E < 20 MeV only account for less than 10% of the total soft Single Event Upsets. It is more significant and reasonable to test the Single Event Upset error rate with a higher energy proton beam. ATLAS recommended the proton energy should be in the range 60 to 200 MeV.

The destructive Single Event Effect is the most severe and dangerous damage a heavy particle could induce to an electronic device. Up-to-date, no study has been conducted to estimate the rates of Single Hard Error and destructive SEEs. However it is clear that the production of hard and destructive SEEs requires a high local instantaneous energy deposition (much higher than that required for producing soft SEUs). In HEP experiments like ATLAS, particles with a high linear energy transfer are produced by fission reactions induced by energetic hadrons on elements heavier than 170-180 AMU. It is estimated that most of the fission reactions can be triggered by 500 MeV protons. A proton beam with the energy 500 MeV or above can be used to test the hard and destructive SEEs.

4 Radiation Tolerance Criteria

ATLAS electronic components must have radiation tolerance equal to or higher than minimum values called Radiation Tolerance Criteria (RTC) of 10 years of LHC operation. The RTCs for Total Ionizing Dose (TID) and Displacement Damage (Non-Ionizing Energy Loss/NIEL) are defined as following:

- $RTC_{TID} = SRL_{TID}SF_{sim}SF_{LDR}SF_{lot}$ (unit: rad/yr),

- $RTC_{NIEL} = SRL_{NIEL}SF_{sim}SF_{LDR}SF_{lot}$ (unit: 1-MeV-equivalent neutrons/cm^2/yr).

where the SRL stands for the Simulated Radiation Level which is introduced in section 2. Table 2 lists the safety factors for various concerns.

The RTCs for Single Event Effects are the SEE error rate. The values have to be defined by each detector system based on an acceptable data loss rate. The radiation tolerance criteria for the CSC system will be discussed in the next section.

Table 2: Safety Factors defined by ATLAS Radiation Tolerance Assurance Group.

Parameter	Description	TID	NIEL
SF_{sim}	Safety Factor for Simulation	4	4
SF_{LDR}	Safety Factor for Low Dose Rate	5	1
SF_{lot}	Safety Factor for unknown lots	4	4

5 Radiation Tolerance Criteria for Single Event Upset

There is no ATLAS-wide Radiation Tolerance Criteria for the Single Event Upset rate up-to-date. For the on detector electronics of Cathode Strip Chamber, we have adopted an in-efficiency of 0.1% for the whole CSC system due to Single Event Upsets. The number is ignorable compared to the in-efficiencies due to other factors. To obtain an acceptable upset rate for a single G-Link chip, we calculate the error rate standard as shown in table 3 based on the test of the G-Link transmitter by the ATLAS Liquid Argon group.

Table 3: Radiation Tolerance Criteria for SEU

Parameter	value	Comment
CSC system in-efficiency	0.1%	In-efficiency is defined as 100% - efficiency
In-efficiency per G-Link	0.78×10^{-6}	1280 weighted G-links for the CSCs †
Link-down time	1 ms	1 ms to recover a link down.
No. of chips per link	2	transmitter and receiver
Data dropped after recovery	8 triggers	8 triggers worth of data will be dropped to flush the garbled charges due to the link down.
Link down probability per SEU	100%	Although not every SEU causes link-down, link-down certainly will introduce more problem. To set a safe SEU rate, we assume the worst for each SEU occurance.
Acceptable SEU rate	one SEU per 43 minutes per chip	A factor of 5 has to be considered to account for the uncertainty in neutron flux simulation.

† The total number of G-Links on detector is 960. 2/3 of them are transmitters and 1/3 of them are receivers. When one receiver link is down, because it is carrying control signals, the two transmitter links on the same ASM board will not transmit any data, so the data loss will be twice as much as when the

transmitter link is down. We give a weight of 2 to the receiver links and a weight of 1 to the transmitter links. Therefore the total weighted G-Links on detector is 1280.

6 Irradiation Test Methods

- TID test method for the qualification of CMOS/bipolar/BiCMOS lots

    1. Selection of a calibrated ionizing dose facility (Gamma or X-ray);
    2. Selection of a set of 11 good devices (for a known lot) or 22 good devices (for unknown lot);
    3. Number all devices;
    4. Electrical measurement of all devices at room temperature;
    5. Random selection of 1 device among the set of 11 (or 2 among the set of 22). The selected devices will not be irradiated and will serve as the reference.
    6. Irradiation of the 10 (0r 20) other devices at room temperature under bias in one or several steps up to the RTC required for CSC.
    7. Electrical measurements at room temperature; rejection of the lot if one of the 10 (or 20) fails;
    8. Annealing of CMOS devices under bias 168 hours at room temperature; rejection of the lot if one device fails;
    9. Documentation of the test result.

- Displacement Damage (NIEL) test method – any device except pure CMOS devices (pure CMOS devices are naturally tolerant to displacement damage).

    1. Selection of a calibrated neutron facility (1-MeV-equivalent neutrons/cm^2).
    2. Selection of a set of 11 good devices (for a known lot) or 22 good devices (for unknown lots);
    3. Number all devices;
    4. Electrical measurement on each device at room temperature;
    5. Random selection of 1 device among the 11 or 2 devices among the 22 as the reference; the Selected device(s) will not be irradiated.
    6. Irradiation of the rest 10 (or 20) devices up to the RTC at CSC; During irradiation, all the leads of each device must be shortened together;
    7. Electrical measurement on each irradiated device at room temperature plus inspection of any damage after deactivation.
    8. Rejection of the generic component if any of the 10 (or 20) irradiated devices fails.

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9. Documentation of test result.

- Single Event Effect(SEE) test method – based on proton beam

  1. Selection of a calibrated proton facility, 60 MeV proton beam for soft SEE test only or >500 MeV proton beam for global SEE test including soft, hard and destructive SEEs.

  2. Selection of a set of 4 good devices from unknown lots.

  3. Number all devices.

  4. Electrical measurements on each device at room temperature (pre-irradiation, check whether on-line monitoring is working properly).

  5. Irradiation of each device at a controlled temperature with a constant proton flux, up to a total fluence large enough to produce an accurate measurement of the SEE rate. During irradiation: on-line electrical operation and measurement.

  6. After irradiation, inspection for destructive damage.

  7. Computation of the soft, hard and destructive SEE rates expected in the ATLAS CSC location.

  8. Documentation of the test result.

7 Electronics devices to be tested for radiation tolerance

Electronic devices mounted on the CSC detector will have to be qualified for radiation tolerance of 10 years of operation. Table 4 lists the devices to be tested.

Table 4: CSC on detector electronics devices to be tested for radiation tolerance.

Component	Function
HDMP 1022	G-Link transmitter
HDMP 1024	G-Link receiver
SCA	Switched-Capacitor Array
AD 9042	Analog Digital Converter
AD 8042	Op-Amp
DAC	Digital Analog Converter
Level Translators	Translator between different logics
Readout interface IC	

8 Irradiation facilities

We have established that the following facilities are suitable for the radiation tolerance assurance tests:

1. The ^{60}Co source at Gamma Irradiation Service at the University of Michigan provides a peak gamma rate of 2 Mrad/hour at the center. This source can be used for the total ionizing dose effect test. Approximately 15 minutes of irradiation will be needed at this source or longer time if the devices under test are irradiated at a lower gamma rate.

2. Nuclear reactor at University of Rhode Island provides 1-MeV-equivalent neutrons at a flux of 4×10^{12} neutrons/cm^2.s. Using this facility, 75 seconds of irradiation will be able to qualify or disqualify a device for the displacement damage effect.

3. Crocker Cyclotron at University of California, Davis provides 63 MeV proton beam. The beam flux can be tuned in the range $3 \times 10^5 \sim 2 \times 10^{10}$ protons/cm^2.s. This facility can be used to test the Single Event Upset.

4. Neutron Science Center at Los Alamos National Laboratory provides 800 MeV proton beam at a maximum flux of 3×10^{12} protons/cm^2.s. This source can be used to test the Single Hard Error, Latchup, Gate Rupture and Burnout. Any of these errors will disqualify a device.

The radiation tolerance of the electronics devices has to be studied very carefully to assure the success of the whole data acquisition system for the Cathode Strip Chamber.

Single Event Upset Studies of a High Speed Digital Optical Data Link

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Abstract

The results from a series of neutron and photon irradiation tests of a high speed digital optical data link based on a commercial serialiser and a vertical cavity surface emitting laser are described. The link was developed as a candidate for the front-end readout of the ATLAS electromagnetic calorimeter. The components at the emitting end of the link were unaffected by neutron and photon irradiation levels exceeding those expected during 10 years of LHC running. However, the link suffered from single event upsets (SEU) when irradiated with energetic neutrons. A very general method based on the Burst Generation Rate (BGR) model has been developed and is used to extrapolate the error rate observed during tests to that expected at the LHC. A model independent extrapolation was used to check the BGR approach and the results were consistent once systematic errors were taken into account.

Key words: Radiation tolerance; Single event upset rate; Gb/s devices; ATLAS
PACS: 29.90.+r; 42.81.-i; 42.88.+h; 85.60.-q

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1 Introduction

The Liquid Argon Calorimeter [1] of the ATLAS experiment at the LHC is a highly segmented particle detector with approximately 200 000 channels. Signals generated by particles impacting the calorimeter are small and sensitive to coherent noise. Information derived from these signals is digitised on the detector and subsequently transmitted to data acquisition electronics situated 100 to 200 metres away. The restricted space available for the signal cables and the need to minimise noise generated by ground loops led to a choice of digital optical links for the data transmission. The front-end electronics has a high degree of multiplexing allowing the calorimeter to be read out over 1600 links each transmitting 32 bits of data at the LHC bunch crossing frequency of 40.08 MHz. A major consideration in the design of the link is the performance in the presence of radiation. The sender part of the link resides in electronics crates which will be exposed to an integrated fluence of 1.7×10^{13} neutrons(1 MeV Si) per cm^2 of the components' surface, an 800 Gy (Si) dose of photons [2] and a three orders of magnitude smaller dose of charged particles over 10 years of LHC running (1 LHC year = 10^7 seconds). These estimates include conservative safety factors.

Early performance tests of the candidate link and irradiation studies are described in Refs. [3] and [4]. The link is based around VCSELs (Vertical Cavity Surface Emitting Lasers) which were chosen for their radiation tolerance [5]. In this paper a more detailed study of the link performance in the presence of neutron and photon radiation is described and the single event upset characteristics are emphasized. Photon radiation has no effect on the silicon based electronic components of the present set-up. Its effect on optical fibres is found to depend on fibre composition [6]. During the neutron irradiation studies of the link, transient data transmission errors have been observed and identified as Single Event Upsets (SEUs) [7]. The rate of observed SEUs is extrapolated to that expected at the LHC. The extrapolation requires a knowledge of the expected neutron spectrum in ATLAS, which is obtained from detector simulations. It also requires that the dependence of the error rate on the incoming neutron energy is understood. Various neutron sources have been used experimentally : a 2.5 MeV neutron generator with a deuteron beam impinging on a deuteron target and cyclotrons with deuteron (proton) beams with tunable energies ranging from 5 MeV (20 MeV) up to 25 MeV (34 MeV) impinging on a beryllium target. Data has been interpreted using two independent methods : 1) the Burst Generation Rate Model [7] and 2) a model independent extraction of the error rate using several neutron beams with different energy spectra.

2 Optical link description

A schematic overview of the demonstrator link is shown in Fig. 1. The demonstrator link is based on an Agilent Technologies[3] HDMP1022/1024 serialiser/deserialiser set (commonly known as 'G-link') [8], a VCSEL emitting light at a wavelength of 850 nm, a GRaded INdex (GRIN) 50/125 μm optical fibre and a PIN diode. The VCSEL and PIN diode were packaged together with driving and discriminating circuits as transceiver modules.
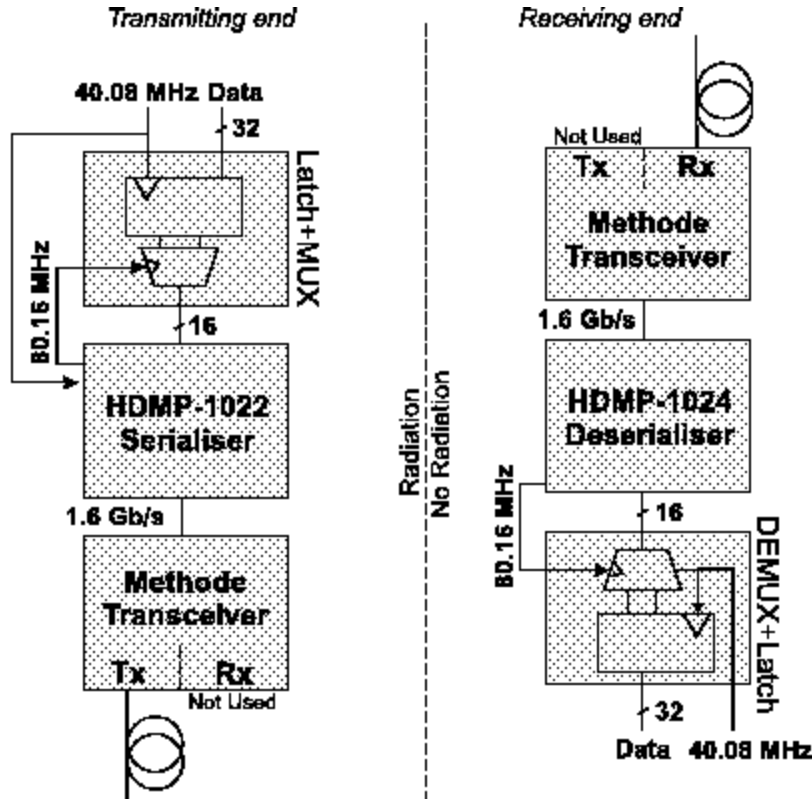
Fig. 1. A Gb/s demonstrator link based on the G-link chipset.

Data is loaded into the G-link serialiser (Tx) and is delivered to the deserialiser (Rx) over a serial channel. The G-link is operated in double frame mode : the addition of external (de)multiplexing elements allows a 32 bit data word to be sent as two 16 bit segments. The G-link chip set provides link-down and single error monitoring through the addition of a 4 bit control field appended to each 16 bit data segment. A 'link-down flag' occurs when the G-link receiver cannot identify a frame to lock onto and a 'single error flag' indicates an illegal control field in the transmitted frame. The control field denotes the data type being sent and contains a 'master transition' which the receiver uses for frequency locking. The addition of the control field results in a total link data rate of 1.6 Gb/s.

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[3] Formally Hewlett Packard.

The monolithic silicon bipolar transmitter and receiver chips are packaged in an aluminium M-Quad 80 package. The G-link transmitter has a PECL serial output and can be connected directly to the input of standard optical transceiver modules. Inside the transceiver modules, the transmitter part consists of a driver circuit coupled to a VCSEL. The receiver contains a PIN photodiode, discriminator and a preamplifier assembly. The transmitter and receiver can be coupled to an optical fibre with an industry standard SC connector.

A Programmable Logic Array (ALTERA EMP7128) is placed on the receiver board to facilitate demultiplexing and to interface error and link-down flags to the data acquisition system. The demonstrator link has been tested successfully in the laboratory and no errors were seen during several months of operation. This result exceeds the specified 10^{-14} bit error rate.

3 Radiation facilities and dosimetry

3.1 Neutron irradiations

The neutron irradiations were carried out at three different places :

- SARA (Grenoble-France) : a detailed description of this facility can be found in Ref. [9]. The neutron source consists of a thick beryllium target, 35 mm in diameter, bombarded with a $5\,\mu$A beam of 20 MeV deuterons. A high neutron flux is obtained via stripping reactions. The neutron energy distributions obtained from d + Be → n reactions are illustrated in Fig. 2a (derived from Ref. [10] with a neutron energy detection threshold of 1 MeV). The mean neutron energy measured at SARA is 6 MeV (the neutron energy detection threshold was 100 keV). During irradiation the link components were mounted on an aluminium plate approximately 30 cm from the target.

  The typical neutron flux experienced by link components was $(2.5\pm0.4)\times 10^{11}\,\mathrm{n\,cm^{-2}\,hr^{-1}}$ or about 2 orders of magnitude larger than that expected at the LHC. Neutron fluences were measured with an accuracy of $\simeq 15\,\%$ using passive monitors based on an activation method [9] using the charge exchange reaction ^{58}Ni(n,p)^{58}Co. The SARA facility is now closed.
- CERI (Orléans-France) : the SARA and CERI neutron production mechanisms and dosimetry are identical but the energy of the incident deuteron (proton) beam is tuneable from 5 MeV (8 MeV) up to 25 MeV (34 MeV) at CERI. Data were taken at the deuteron beam energies of 5, 7, 14, 20 and 25 MeV (20, 25, 30 and 34 MeV). The neutron energy distributions obtained from d + Be → n (p + Be → n) reactions are illustrated in Fig. 2a (Fig. 2b - derived from Ref. [11] where a neutron energy detection thresh-
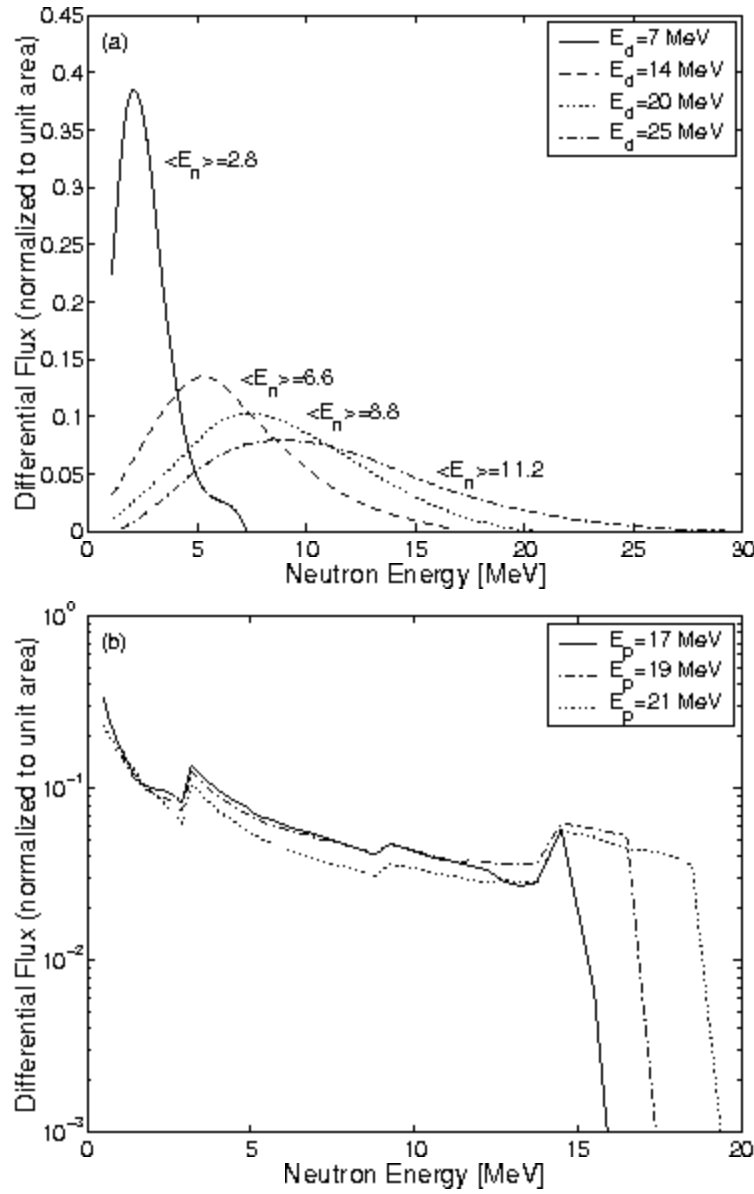
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Fig. 2. The neutron energy spectra obtained from (a) d + Be → n for various incident deuteron beam energies (this figure is derived from Ref. [10] and the neutron energy detection threshold is 1 MeV) and (b) p + Be → n for various incident proton beam energies (this figure is derived from Ref. [11] and the neutron energy detection threshold is 500 keV).

old of 500 keV was applied). The irradiated components were placed 10 cm from the target. The CERI neutron flux was kept constant while the incident beam energies were varied and was identical to that used at SARA : $(2.5 \pm 0.4) \times 10^{11} \, \mathrm{n \, cm^{-2} \, hr^{-1}}$. This was achieved by taking the neutron yield (n/nA sec sr) distribution as a function of the incident beam energy from Refs. [9] and [12]. At a fixed incident beam energy the neutron flux is proportional to the incident beam current.

- Chalmers (Göteborg-Sweden) : the neutron source comprises of a deuteron

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beam impinging on a deuteron target producing essentially monoenergetic neutrons of energy 2.5 MeV. The Chalmers neutron flux was $3.6 \times 10^9 \mathrm{n\,cm^{-2}\,hr^{-1}}$. The neutron fluences were measured using a calibrated neutron counter placed 1 m from the target.

3.2 *Gamma irradiations*

The gamma irradiations were performed at Karolinska Hospital [3] in Stockholm using a ^{60}Co source with gamma ray emissions at 1.17 MeV and 1.33 MeV. The delivered dose was approximately $80 \mathrm{\,Gyh^{-1}}$. Polymer analine dosimeters were fixed onto the components under test. Doses could be measured with an accuracy of $\simeq 4\,\%$.

4 Testing procedure and results

4.1 *Experimental procedure*

Several link sender boards (see Fig. 1) were exposed to both neutron and gamma fluxes to assess the radiation tolerance of the G-link serialiser and different commercial transceivers. No additional link elements e.g, the multiplexer, were exposed to the radiation. A development in a qualified radiation tolerant technology is envisaged for the multiplexer.

During irradiation tests, the behaviour of the link was monitored on-line using the G-link's inbuilt error detection functionality (see section 2). Two different aspects were investigated : the sender part of the link must withstand a total neutron fluence equivalent to 10 years of LHC running (total dose studies) and the radiation induced bit error rate in the link must be acceptable (transient error rate studies).

4.2 *Results of the neutron irradiation tests*

The neutron total dose studies of the link components demonstrated that the G-link serialiser withstands doses of 5×10^{13}(1 MeV Si) neutrons/cm^2 which corresponds to about 40 years of LHC running. Among the commercial LAN transceivers tested only those produced by Methode Electronics Inc. tolerated such neutron doses. More details concerning these tests can be found in Refs. [3] and [4].

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The online link performance tests showed that transient errors ('single' or 'linkdown' error flags) occurred under neutron radiation. For a fixed neutron flux the error rate depended on the average energy ($<E_n>$) of the incoming neutron beam (see Fig. 3a). A test carried out at the Chalmers facility showed that 2.5 MeV neutrons induce no errors in the link indicating that the process generating errors has a threshold at a neutron energy greater than 2.5 MeV.

The error rate dependence with the neutron flux was demonstrated at the SARA facility by varying the intensity of the incident deuteron beam. This result is shown in Fig. 3b.

4.3 Results of the gamma irradiation tests

The radiation tolerance of the sender part of the link has been tested up to a total dose of 800 Gy (Si). Additionally the G-link chip was exposed up to 3000 Gy (Si), which corresponds to 40 years of LHC running. Unlike the neutron irradiation tests, no transient errors of any kind were observed.

5 Neutron induced single event upset analysis

5.1 Error causing processes.

There are many possible sources of radiation induced transient errors in silicon based electronics. The most common ones are due to the passage of ionising particles through the sensitive volume of the device [13] [14]. Charged particles can be produced through a number of nuclear reactions induced by neutrons :
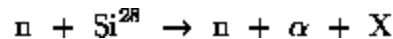
- recoil nuclei from elastic neutron scattering :

$$n + Si^{28} \rightarrow n + Si^{28}$$
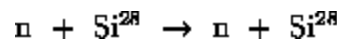
- inelastic reactions producing protons and alpha particles :

$$n + Si^{28} \rightarrow p + Al^{28}$$
$$n + Si^{28} \rightarrow \alpha + Mg^{25}$$
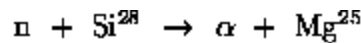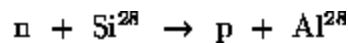
- nuclear fragmentation :
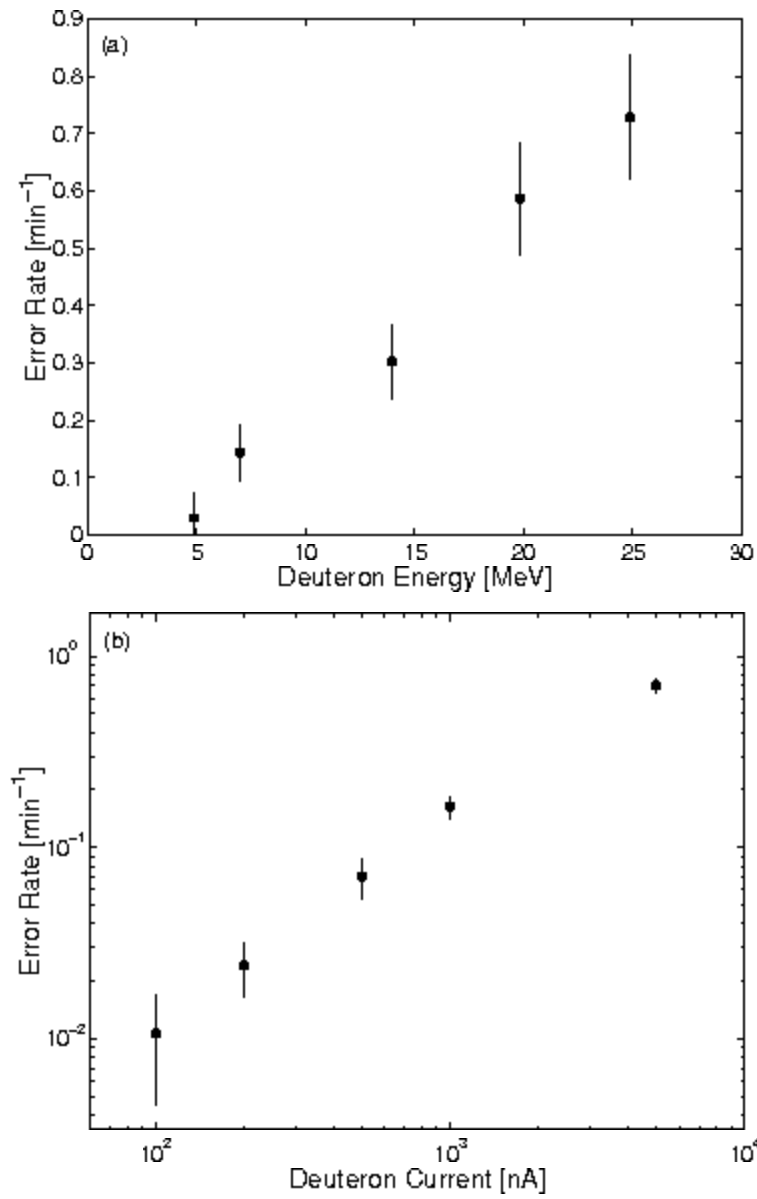
$$n + Si^{28} \rightarrow n + \alpha + X$$

and others.

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Fig. 3. The transient error rate (a) at a fixed neutron flux $((2.5 \pm 0.4) \times 10^{11}\,\mathrm{n\,cm^{-2}\,hr^{-1}})$ as a function of the incident deuteron beam energy ($<E_n>$ scan), and, (b) at a fixed deuteron beam energy (20 MeV) as a function of the incident deuteron beam current (which is proportional to the neutron flux), the 5 μA measurement corresponds to a nominal flux of $(2.5 \pm 0.4) \times 10^{11}\,\mathrm{n\,cm^{-2}\,hr^{-1}}$.

The (n,n), (n,α) and (n,p) reactions are dominant [7] for neutrons with an energy smaller than 20 MeV. For higher energy neutrons, inelastic scattering (n,n') and reactions such as (n, n' p) and (n, n' α) dominate. The cross sections for p and α production in silicon as a function of the neutron energy are illustrated in Fig. 4.

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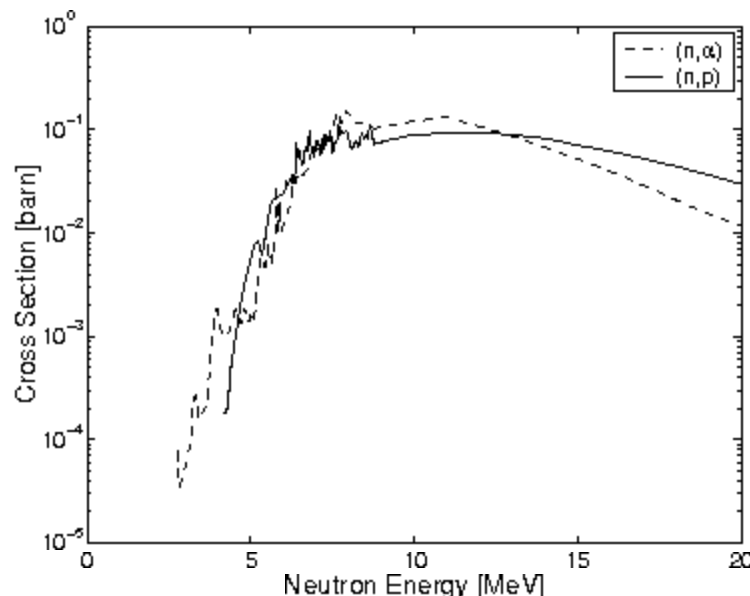
Fig. 4. The cross sections for p and α production in silicon, $n + Si^{28} \rightarrow p + Al^{28}$ and $n + Si^{28} \rightarrow \alpha + Mg^{25}$, as a function of the neutron energy [15].

The main parameters that need to be taken into account in order to estimate the SEU rate are the sensitive volume of the chip under test and the critical energy which needs to be deposited within the sensitive volume to create upset.

The interaction of a neutron with silicon produces a shower of secondary particles in the chip and a nuclear recoil or in some cases several fragments. The probability that a charged particle emerging from the collision will traverse a sensitive section of the electronic device depends on the distance from the production point. To produce a SEU typically requires energy deposition exceeding a few hundred keV. Due to kinematic considerations, no SEU is expected for neutrons with an energy below $\simeq 2.5$ MeV (see section 4.2 and Ref. [14]), except for a possible effect due to the interaction of thermal neutrons with boron ($^{10}B(n,\alpha)^{7}Li$) dopants in the chip. However, the conclusions of recent studies published in Ref. [14] state that thermal neutrons do not play an important role in SEU at the LHC when compared with the effects induced by higher energy neutrons.

5.2 Burst Generation Rate model

Neutrons interacting with silicon produce ionising recoils from nuclear reactions of the type (n,n), (n,p) and (n,α). These reactions and the energy deposition they induce can be analysed in terms of the "Burst Generation Rate" (BGR) model [13]. This model has been defined in terms of a partial macroscopic cross section ($BGR(E_n, E_r)$) for neutrons of energy E_n to produce recoils of energy E_r or greater. This cross section can be applied to the

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differential neutron energy spectrum (dN/dE_n) to estimate the SEU rate. The BGR method of calculating the rate of neutron-induced SEUs due to recoils has been shown to be effective [16] in other applications.

The definition given in Ref. [7] has been used in the present analysis :

$$\frac{d\,SEU}{dt} = V \times C \times g \times \int_{E_n} BGR(E_n, E_r) \times (dN/dE_n)dE \qquad (1)$$

Here, V is the sensitive volume of the chip (μm^3), C is the collection efficiency (fraction of charge released by the recoil collected in V : upset/recoil) and g is an additional correction factor (e.g., to account for contributions from light ions). Note that the product $V \times C \times g$ only depends on the intrinsic parameters of the device under test. Consequently, it can be extracted as a constant factor from the experimental data.

5.3 Application to the CERI experimental data

The BGR model applied to the CERI like neutron spectra ($d + Be \rightarrow n$ and $p + Be \rightarrow n$) implies that the integral :

$$I_{BGR} = \int_{E_n} BGR(E_n, E_r) \times (dN/dE_n)dE$$

is proportional to the measured error rate at CERI.

In the present analysis, the $BGR(E_n, E_r)$ functions illustrated in Fig. 5 are taken from Ref. [16]. To perform the I_{BGR} calculation they are combined with the differential neutron energy spectra taken from Refs. [10], [11] and [17]. The neutron spectrum produced by $p + Be \rightarrow n$ interactions with $E_p = 34$ MeV is measured at the CERI facility [18]. In the I_{BGR} calculation the neutron spectra detailed above are normalized to unit area.

The χ^2 dependence of the recoil energy E_r in a linear fit of the measured SEU rate ($d + Be \rightarrow n$ and $p + Be \rightarrow n$ CERI experimental data) versus I_{BGR} is shown in Fig. 6. The optimal value of E_r (denoted E_{opt}) where the χ^2 minimises is $E_{opt} = 0.5 \pm 0.4$ MeV.

In Fig. 7, the SEU upset rates recorded during CERI experiments are compared with the results of previous BGR calculations for $E_r = E_{opt}$. The two sets of CERI measurements (and the respective BGR model calculations) are plotted together : $d + Be \rightarrow n$ with E_d ranging from 5 MeV (2.6 MeV) up to

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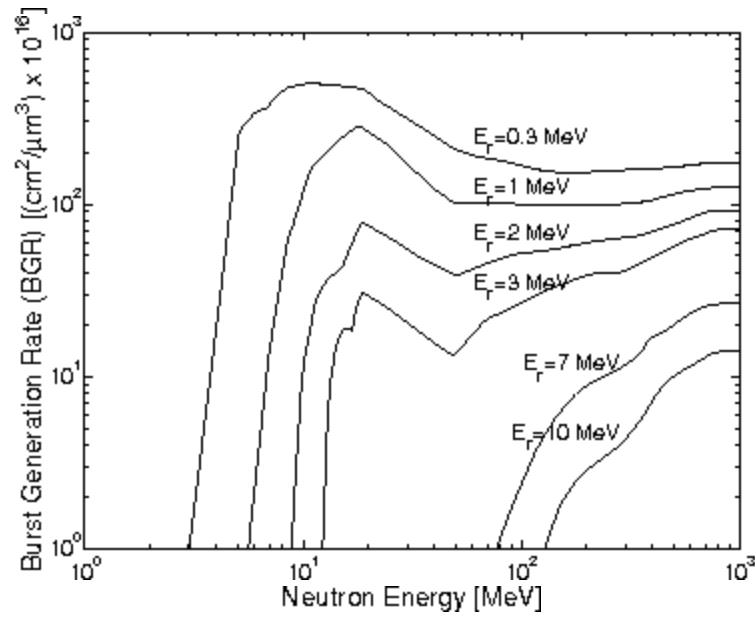Fig. 5. BGR(E_n,E_r) functions for neutrons of energy E_n creating recoils of energy E_r or greater [16].
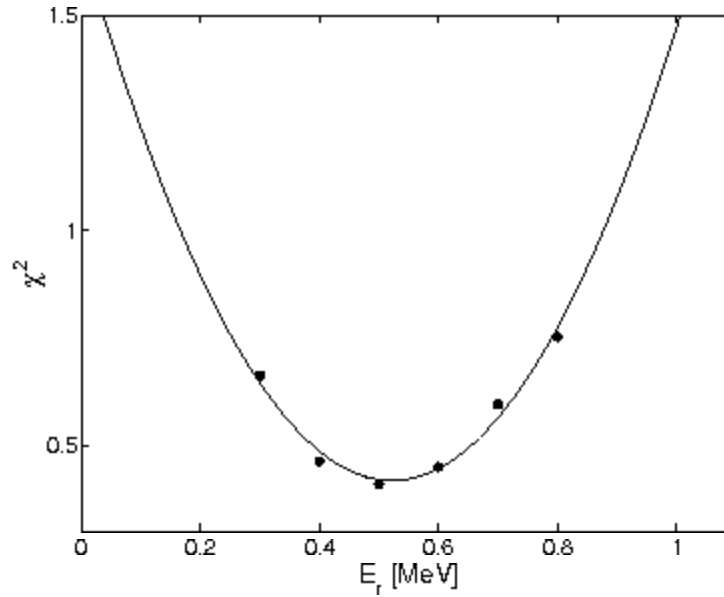

Fig. 6. Results from a χ^2 analysis to determine the optimal value of E_r from a linear fit of the CERI SEU rate measurements (d + Be → n and p + Be → n) versus I_{BGR}.

25 MeV (24 MeV) and p + Be → n with E_p ranging from 20 MeV (17 MeV) up to 34 MeV (34 MeV).

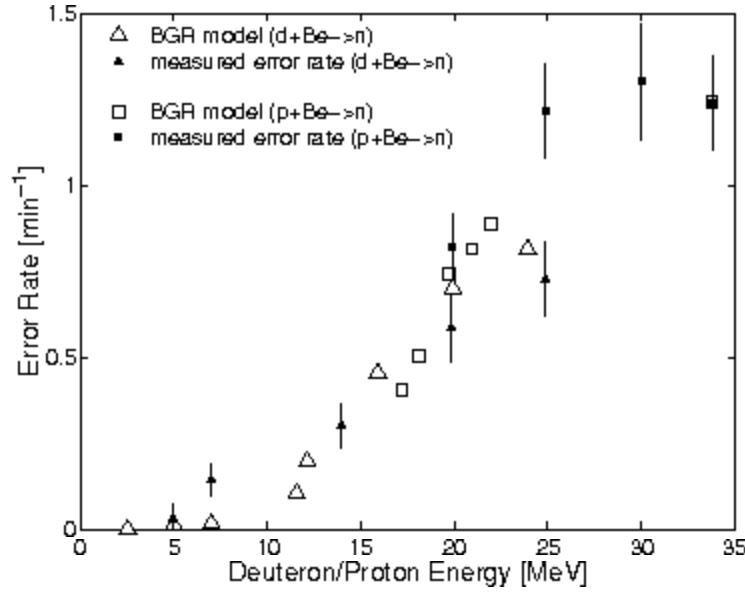The model and the experimental results are in close agreement.

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Fig. 7. Two sets of CERI measurements (d + Be → n and p + Be → n) plotted together with the respective BGR model calculations for the optimal value of the BGR recoil energy parameter ($E_r = E_{opt}$).

6 Single event upset rate estimate in ATLAS

6.1 ATLAS like conditions
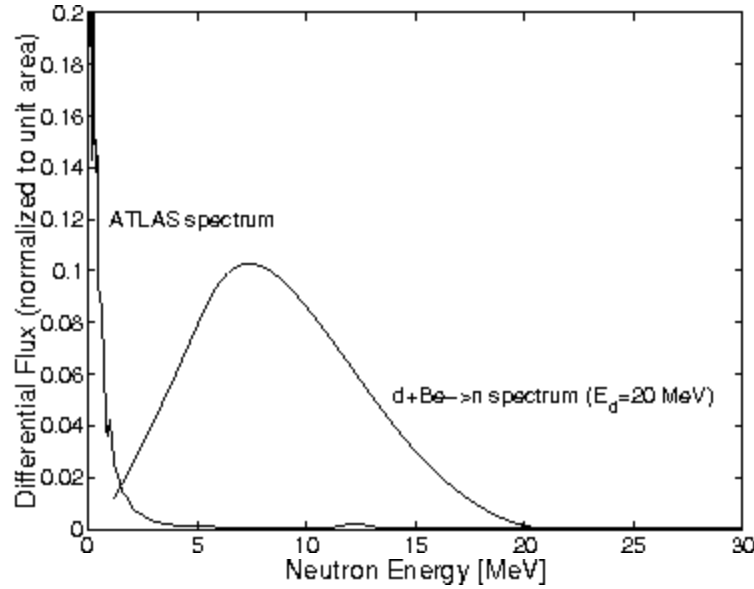
Fig. 8. A comparison of the ATLAS neutron energy spectrum with the experimental spectrum corresponding to d + Be → n and $E_d = 20$ MeV. The curves are normalized. The ATLAS neutron spectrum peaks strongly at low energies and so the y-axis is truncated at 0.2.

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The aim of this study is to extrapolate the SEU rate measured at the neutron irradiation facilities to that expected in ATLAS during the running of the experiment. The differences between the expected neutron fluxes and energy spectra must be accounted for.

There are independent calculations of the expected neutron flux in ATLAS [2,19], [20]. The predictions of the total neutron flux agree and differences in the detailed spectral shapes can be ascribed mainly to differences in the modelling of the detector. The estimated total neutron flux at ATLAS is two orders of magnitude lower than at CERI [19], [20].

The neutron energy spectrum calculated for the location of calorimeter electronics crates is shown in Fig. 8 together with a representative experimental neutron test spectrum. In this study, the portion of the neutron spectrum below 2.5 MeV has been neglected since an apparent threshold for the SEUs (see section 4.2) has been observed. For a 20 MeV deuteron beam at CERI approximately 85 % of the neutron energy spectrum is above 2.5 MeV. In ATLAS this percentage is significantly lower : 14 ± 9 % [19], [20].

6.2 Application of the BGR method

In equation (1) the CERI-like neutron spectra are replaced by that expected in ATLAS [19]. The product $V \times C \times g$ has been deduced from analysis of CERI data for each E_r value in the range $E_{opt} = 0.5 \pm 0.4$ MeV.

Using the BGR method the ATLAS error rate is estimated at 0.005 ± 0.003 error/link/hour. This results only takes into account the G-link in-built error flags. A refined CERI test where the content of data words was checked led to an estimate of 0.013 ± 0.006 error/link/hour. This value is multiplied by a safety factor of 5 to take into account the uncertainties in the simulation of the ATLAS neutron spectrum [2]. Consequently the expected error rate is 0.065 ± 0.030 error/link/hour.

6.3 Model independent extraction of the error rate

The BGR model depends on a large number of assumptions about the processes contributing to the SEU rate and about the composition of the chip under test. During the irradiation tests, SEU rates were measured using neutrons generated by deuterons and protons beams at several different energies but with an identical neutron flux. For each incident beam energy the neutron energy spectrum spanned different, and often overlapping, ranges. This allows the probability for a neutron of a given energy to generate SEU to be

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derived directly from data. For each CERI incident beam energy (E_{beam}), the measured error rate, N_i(error), is given by an integral of the product of the probability for a neutron at a given energy to produce an error over the neutron energy spectrum :

$$\int_{E_n} P(E_n) \times (dN/dE_n)_i dE = N_i(error) \tag{2}$$

Here, P is the probability for a neutron of energy E_n to create an error and $(dN/dE_n)_i$ is the differential neutron flux (n/cm^2 sec MeV) associated to each E_{beam} value. In the present analysis only seven CERI measurements out of nine were used (i=1,..,7). The p + Be $\rightarrow$ n SEU measurements with E_p = 25 MeV and 30 MeV were excluded since no differential neutron flux data was available. As in the BGR model analysis, the neutron spectra used in this analysis were normalized to unit area and taken from Refs. [10], [11], [17] and [18](E_p = 34 MeV).

The neutron energy range spanned by the seven CERI measurements can be divided into seven bins in order to extract the values of P_j, defined as the probability for a neutron in the $(\Delta E_n)_j$ energy range to create SEU :

$$P_1 : \qquad\qquad E_n \leq 3.5 \text{ MeV}$$
$$P_2 : \quad 3.5 \text{ MeV} < E_n \leq 7.0 \text{ MeV}$$
$$P_3 : \quad 7.0 \text{ MeV} < E_n \leq 10.0 \text{ MeV}$$
$$P_4 : 10.0 \text{ MeV} < E_n \leq 14.0 \text{ MeV}$$
$$P_5 : 14.0 \text{ MeV} < E_n \leq 20.0 \text{ MeV}$$
$$P_6 : 20.0 \text{ MeV} < E_n \leq 26.0 \text{ MeV}$$
$$P_7 : 26.0 \text{ MeV} < E_n$$

The equation (2) can be rewritten as a sum over each $(\Delta E_n)_j$ energy range defined above :

$$\Sigma_j P_j \times \int_{(\Delta E_n)_j} (dN/dE_n)_i dE = N_i(error) \tag{3}$$

and recast as a matrix product :

$$M \times P = N \tag{4}$$

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where M is the square matrix (7×7) associated with the coefficients $m_{i,j}$:

$$m_{i,j} = \int\limits_{(\Delta E_n)_j} (dN/dE_n)_i dE$$

and P and N are the vectors associated to P_j and $N_i(error)$, respectively.

From equation (4) the P_j values (j ranges from 1 to 7) can be deduced.

Using a procedure similar to that described for the BGR method (see section 6.1), the ATLAS neutron energy spectrum is used in equation (3) where i now equals 1 and an ATLAS like error rate is extracted : 0.018 error/link/hour. As for the BGR calculations, this value should be multiplied by a safety factor of 5 to account for uncertainties on the ATLAS neutron energy spectrum. Consequently, the expected error rate is 0.090 errors/link/hour which is compatible with the BGR model prediction of : 0.065 ± 0.030 error/link/hour.

6.4 Discussion

The results obtained from the two methods described in the previous sections are consistent. The BGR method leads to an expected SEU rate in ATLAS of 0.065 ± 0.030 error/link/hour (including a conservative safety factor of 5). The technique to measure and then to extrapolate to ATLAS-like conditions is general and does not depend on the detailed composition of the electronics component under test.

In the G-link based set-up, a large fraction (about 50 %) of the SEUs results in a loss of synchronisation between the serialiser and deserialiser chips (a 'link-down error'). The re-synchronisation of the chip set can take up to few milliseconds. All information transmitted during this time is lost. An ATLAS SEU rate of 0.065 ± 0.030 error/link/hour implies a dead time of the order of 10^{-5} for the entire calorimeter (1600 links). To reduce this number, a possible solution for ATLAS is a dual G-link system carrying identical information on two independent links and a fast switch on the receiving end selecting the uncorrupted data. In such a design, the probability for two links to be down due to SEU at the same time is negligible.

7 Conclusions

A 1.6 Gb/s demonstrator link based on the commercial G-link chipset has been built and tested in a neutron and gamma radiation environment. The

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components have been found to be radiation tolerant at least up to 1.7×10^{13} n (1 MeV Si) cm^{-2} and 800 Gy gamma radiation which corresponds to 10 years of LHC running including safety factors [2]. No adverse effects have been observed during gamma irradiations up to 3000 Gy using a ^{60}Co source. The radiation tolerance of a G-link serialiser coupled to a Methode transceiver has been also demonstrated under neutron radiation up to 5×10^{13} (1 MeV Si) neutrons/cm^2.

Transient errors were observed during neutron irradiations, but none were seen during gamma irradiations. Two different approaches have been used to estimate the single event upset rate in ATLAS-like conditions. The first is based on the Burst Generation Rate (BGR) model and leads to an ATLAS error rate of 0.065 ± 0.030 error/link/hour (including a safety factor of 5 to account for uncertainties in the ATLAS neutron spectrum [2]). A simple matrix inversion method based on experimental data confirms the BGR method estimate of ATLAS single event upset rate. The BGR model method is general and could be used to study the single event upset rate for any type of electronic set-up.

8   Acknowledgements

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DEVELOPMENT OF RADIATION TOLERANT Gb/s OPTICAL LINKS FOR THE FRONT-END READOUT OF THE ATLAS LIQUID ARGON CALORIMETER

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Abstract

In the baseline readout solution for the ATLAS liquid argon calorimeter, approximately 1500 unidirectional Gigabit/s (Gb/s) fibre-optic links are used to transfer data from the calorimeter to receivers in data acquisition electronics situated up to 200 m away. In an architecture currently under study, 'G-Link' seraliser chips manufactured by Hewlett Packard are used to convert calorimeter data words into a 1.6 Gb/s serial data stream which is fed into a VCSEL (vertical cavity surface emitting laser diode) based emitter system operating at 850 nm. Graded index multimode optical fibres are used to couple the on-detector emitters to PIN-photodiodes located in receivers. In this note results from neutron irradiations of a complete G-Link based link demonstrator are presented along with results from neutron and ionising irradiations of potential link components (packaged VCSEL's and graded-index fibres).

1 INTRODUCTION

1.1 Link Architecture

Approximately 1500 unidirectional optical interconnects are required for the readout of the ATLAS liquid argon (LArg) calorimeter [1]. Each on-detector front-end board (FEB) is fed by 128 'raw' calorimeter channels which are processed and on receipt of a level-1 trigger accept readout over an optical interconnect. The interconnect must allow a throughput of 1.28 Gb/s (32 bits every 25 ns). The bit error rate (BER) of the interconnect must be better then 10^{-9} so the performance of the LArg data acquisition as a whole is not compromised. The interconnect architecture currently favoured is a single serial optical link per FEB as this reduces cost due to the fewer number of components required compared to a parallel link implementation. The link is based around commercial 'off-the-shelf' components. The emitting end of the link comprises of a Hewlett Packard G-Link seraliser chip connected to a VCSEL laser diode [2]. Graded index multimode (50/125) fibre is used to connect the emitters to off-detector receiver
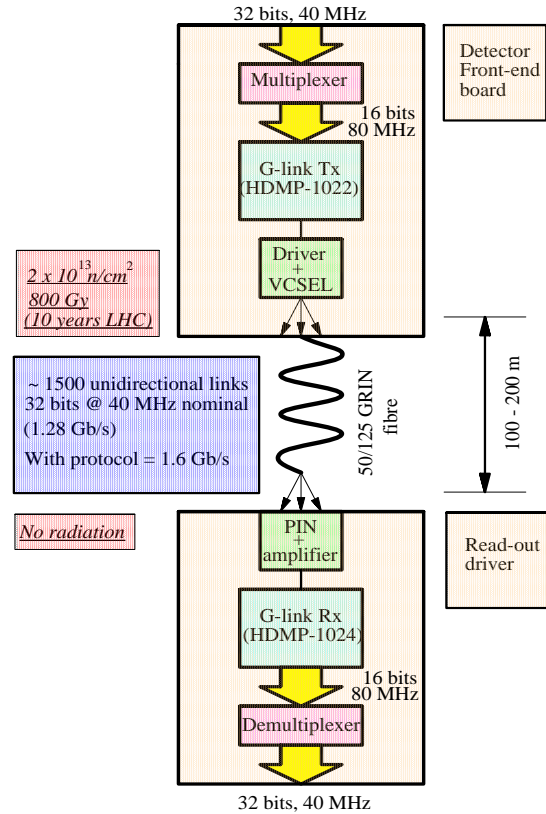

Figure 1: A schematic of the front-end readout links for the ATLAS LArg calorimeter.

units which contain G-Link deseralising chips. This architecture is shown schematically in figure 1.

1.2 Radiation Issues

Over 10 years of LHC running, the components at the emitting end of the link will be subject to high levels of both neutron (1.7×10^{13} n(1 MeV Si) cm^{-2}) and ionising (gamma) radiation (800 Gy). The receiving part of the link is not exposed to significant levels of radiation. Access to link components mounted on-detector would require a lengthy access into ATLAS and so it is important that the

components operate reliably for 10 years in this hostile environment.

Components were irradiated with 6 MeV neutrons at the SARA cyclotron facility in Grenoble [3]. The neutrons are produced by impinging 20 MeV deuterons on a beryllium target. The components under irradiation are located approximately 30 cm from the target, behind a liquid nitrogen cryostat which is used for other tests. The activation of nickel foils was used to determine the absolute neutron fluence to an accuracy of around 15%. The typical neutron flux at SARA is approximately 5×10^{11} n cm^{-2} hr^{-1}, about 1500 greater than that expected in ATLAS.

The gamma irradiations were performed with ^{60}Co facilities at BNL, Brookhaven (only fibre) and Karolinska Hospital, Stockholm (fibre and VCSEL's). As the ^{60}Co source decays it emits two gamma rays at energies of 1.17 MeV and 1.33 MeV. Polymer-alanine dosimeters were used to measure the total ionising dose received by the components under test to an accuracy of around 4%. Solid state detectors were used to cross-check the result. The dose rate delivered at BNL (Karolinska) is approximately 200 (80) Gy hr^{-1}, about 10^4 (4000) greater than that expected in ATLAS.

2 IRRADIATION STUDIES

2.1 Demonstrator Link

Overview

A set of demonstrator links based around the G-Link chipset have been constructed and the emitting end of the link irradiated with neutrons. Both emitter and receiver boards do not have the optics mounted directly. Instead, there is a socket following the industry standard for transceiver modules. This allows a variety of different optical solutions to be easily evaluated - such as a driver circuit (if necessary) coupled to the VCSEL's described in section 2.2. The receiver board also features an Altera PLD to allow some processing of the G-Link outputs. During the tests described in the remainder of this note, industry standard VCSEL-based Gb/s transceiver modules have been used. As the links are unidirectional only half a transceiver is used at either end of the link. Due to this partial use, it is unlikely that such transceivers will be a final solution for ATLAS. However, in a demonstrator link they are very suitable for gaining experience with the irradiation of Gb/s link components.

G-Link Chipset

The G-Link chipset enables parallel data loaded into the transmitter to be delivered to the receiver over a serial channel. The chipset is particular attractive as it hides the complexities of encoding, multiplexing (transmitter) and clock extraction, demultiplexing and decoding (receiver) from the user. Furthermore, frame synchronisation and DC balance are maintained automatically. The G-Link protocol attaches a 4 bit control word to every 16 bit data word sent over the link, making a 20 bit frame, as shown in figure 2. The control word denotes the data type being sent (control, data or fill frame) and contains a 'master transition' which the receiver uses for frequency locking. The chipset is run
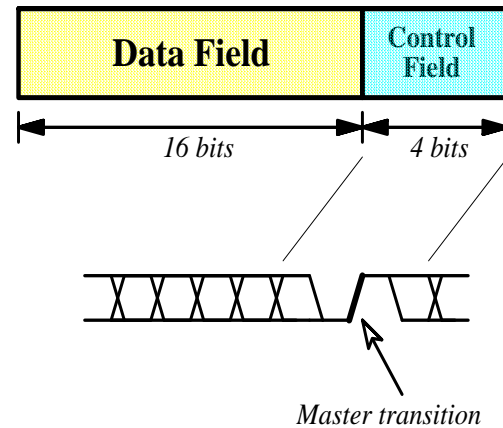

Figure 2: The structure of a G-Link data frame. A 16 bit data word is followed by a 4 bit control word containing a master transition which the receiver uses for frequency locking.

in the 'double frame mode' which, with the addition of external (de)multiplexing elements, allows a 32 bit data word (40 bit frame) to be sent as two separate 20 bit frame segments. Data inputs to the chip are TTL and the serial Gb/s output is PECL. The (de)multiplexing elements are standard ATLAS components, used by many subdetectors, and not expected to present any additional radiation tolerance issues. The monolithic silicon bipolar G-Link chipset is based on a masked 'sea of gates' architecture using 25 GHz transistors.

Transceiver Modules

The transceiver modules contain a 850 nm VCSEL emitter and driver packaged together with a PIN-diode based receiver and amplifier and discriminator. Optical connections are made with push-fit 'SC' connectors. The modules accept PECL inputs and so can be directly coupled to the output of the G-Link. Three varieties of transceiver have been tested : Hewlett Packard, Honeywell HFM2450 and Methode MDX-19-4-1. The Hewlett Packard and Honeywell transceivers use silicon bipolar laser drivers whereas the Methode driver is based on discrete components.

Testing Procedure

The neutron irradiations have two aspects. Firstly, the components on the emitting end of the link must survive

the total neutron fluence expected after 10 years of LHC running without any effect on the performance of the link - total dose studies. Secondly, the radiation induced bit error rate in the link must be acceptable - single event studies. During irradiation all components were biased and approximately 70 m of fibre joined the emitter to the receiver.

A figure of merit describing the performance of a link is traditionally given by the bit error rate. Performing industry standard bit error rate tests at Gb/s speeds requires the use of expensive equipment which is often not optimised for the transfer of 32 bit data words. Moreover, only a single link can be tested at once, which is not ideal for irradiation studies when larger sample sizes are desirable. A purpose built bit error rate tester is under construction for testing LArg links but was not available at the time of the irradiations. For the tests described in this note a simpler approach was followed. Before and after (up to a week afterwards due to a 'cool down' period) an irradiation, the integrity of a single link could be assessed using a logic analyser comparing received data to a reference table. The single link limitation and large dead-time of this method makes it unsuitable for irradiation tests. A simpler scheme, using the G-Link's inbuilt error detecting functionality, is therefore used. The G-Link receiver provides an error flag which is generated internally from a check of the control field in the transmitted frame. The control field check is sensitive to illegal control words (not all 2^4 combinations are allowed) and deviations from a strict alternation of the master transition bit. The data word is not checked. There is also a 'link-down' indicator which is asserted when the G-link cannot identify a frame to lock on to. It is important to understand the frequency of this type of error during irradiation as the G-link error recovery procedure takes a minimum of 128 frames (1.6 μs) to recover the link.

With no radiation present, both tests indicated no errors during many days of operation.

Total Dose Studies

Total dose studies were made in three separate tests, as summarised in table 1. In the first and last tests, the G-Link chips were coupled to transceiver modules. In the second test, the link was run at 160 Mb/s over 15 m copper links. This is discussed further in the next section. In all cases the G-Link chips survived the irradiation with no errors being indicated during the two test procedures described above (using fresh transceivers). Note that G_{1-4} survived a 30 year LHC equivalent irradiation. The only transceiver modules not to suffer damage during irradiation were those supplied by Methode. A post-irradiation 'autopsy' on the Honeywell transceivers revealed that the laser driver had failed but the VCSEL still functioned within specifications when coupled to a fresh driver. The Methode transceiver had a driver comprised of discrete components. For technical reasons, the HP transceiver could not be easily tested after dissection.

Test	G-Link	Optics	G_n status	Optics status
1	G_1	HW_1	OK	Dead
(10	G_2	HW_2	OK	Dead
years	G_3	HP_1	OK	Erratic
equiv.)	G_4	M_1	OK	OK
2	G_1	Cu	OK	n/a
(20	G_2	Cu	OK	n/a
years	G_3	Cu	OK	n/a
equiv.)	G_4	Cu	OK	n/a
3	G_1	M_2	OK	OK
(10	G_5	M_3	OK	OK
years	G_6	M_4	OK	OK
equiv.)	G_7	M_5	OK	OK

Table 1: Summary of G-Link (G_n) demonstrator link irradiations. G-Links G_{1-4} and G_{5-7} come from different batches. Transceivers are denoted by : HW_n, Honeywell; HP_n, Hewlett Packard; M_n, Methode. Test 2 used copper (Cu) links, with the link running at 160 Mb/s.

Single Event Studies

Four complete links equipped with Methode transceivers were used to investigate single event effects during a neutron irradiation. During irradiation, the link-down time was estimated by monitoring the G-link error flag and link-down indicator. The distribution of the link-down times can be seen in figure 3. The sharp peak around zero (12.5 ns)
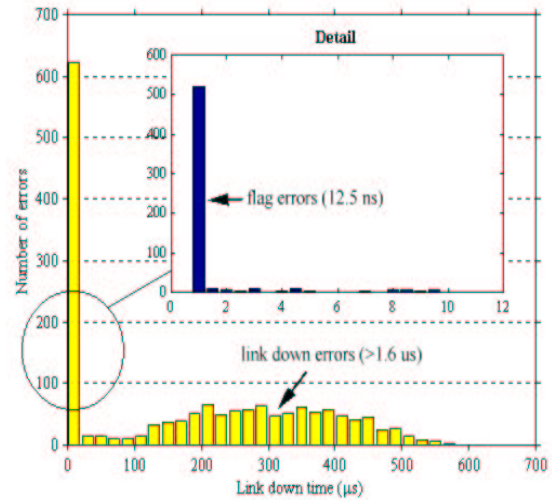

Figure 3: The distribution of the link-down time measured during neutron irradiation for a link comprising G-link chips and Methode transceivers.

is composed solely of error flag errors. The rest of the entries (all >1.6 μs) occur when the G-link asserts the link-down indicator after loosing frame lock. Note that a single link-down event lasting 300μs corresponds to the loss of 24 000 20 bit frames, which is clearly unacceptable. In order to maintain a bit error rate of $\mathcal{O}(10^{-9})$, approximately

one such 300μs link-down event can be tolerated every 100 hours.

The majority of this data was taken at a SARA deuteron beam current of 5 μA which corresponds to a neutron dose rate approximately 1500 that expected in ATLAS. At 5 μA there was approximately 1.5 (1) link-down (error-flag) error recorded per minute. To estimate the error rate at ATLAS-like dose rates, some data was also taken at lower beam currents. The error rate was observed to drop rapidly with beam current, but insufficient beam time was available to allow any robust conclusions to be drawn.

Future tests will be dedicated to low dose-rate studies and improved monitoring of the G-Link error flags will allow the link integrity at ATLAS-like dose rates to be determined. As single event type errors were also observed in the low speed test with copper links (see total dose section), it would be instructive to separate the G-Link and transceiver in a high speed test. As it is impossible to do this with copper links, there is a development under way to drive VCSEL's directly from the G-Link.

2.2 Packaged VCSEL's

Nine Honeywell HFE4080-321 and nine Mitel 1A440 VCSEL's were irradiated with both neutrons and gammas [5]. The VCSEL chips were housed in TO-46 packages encapsulated into metal ST assemblies to allow simple fibre connections. The Honeywell VCSEL's were equipped with plastic lenses to facilitate efficient fibre coupling, the Mitel VCSEL's had a flat window. The active VCSEL chips are approximately cubic with sides of length 500 μm. Similar VCSEL's are used in the transceiver units discussed in section 2.1. During the irradiations the aim was to investigate radiation induced attenuation of the VCSEL's light output and possible changes in the VCSEL's threshold current. As such, the tests purely investigated the DC (time averaged) characteristics of the VCSEL's. Each VCSEL was equipped with a fibre which was routed away from the radiation beams to a PIN-based receiver unit [4] connected to an ADC mounted inside a PC. During irradiation, the VCSEL's were biased above threshold. At periodic intervals the bias current was varied between 0 mA and 10 mA and the corresponding light output recorded. After the irradiation period was over the VCSEL's remained biased to check for any evidence of annealing effects. The total neutron fluence received by the VCSEL's was measured to be $(2.1\pm0.4)\times10^{13}$ n(1 MeV Si) cm^{-2}, corresponding to 10 years of LHC running, and the total ionising dose was (5.1 ± 0.2) kGy, corresponding to 66 years of LHC running.

Figure 4 shows the relative attenuation in the light output from a Honeywell VCSEL as a function of the time during neutron irradiation. The vertical lines denote the start and end of the irradiation period. This plot is typical for all the Honeywell VCSEL's tested and compatible behaviour is seen for all the Mitel VCSEL's. Figure 5
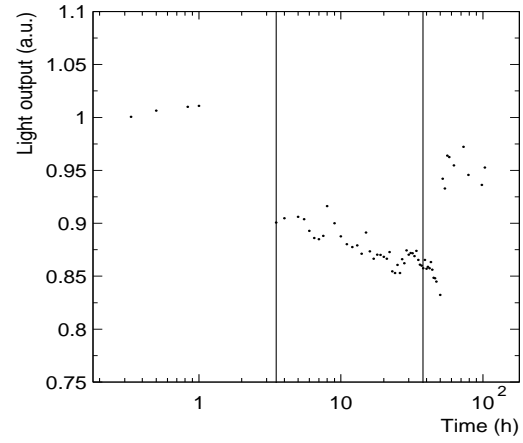

Figure 4: Relative attenuation of the light output from a Honeywell VCSEL as a function of the time during a neutron irradiation. The vertical lines indicate the start and end of the irradiation period. Note the annealing behaviour after the irradiation is completed.

shows the corresponding results from a gamma irradiation. The neutron (gamma) irradiation reduces the light output by about 10% (5%) for 10 year LHC equivalent exposures. After the neutron irradiation a few days of annealing restores the light output to pre-irradiation levels. No such annealing behaviour is observed after the gamma irradiation. The threshold current for either type of VCSEL did not move significantly during either type of irradiation.
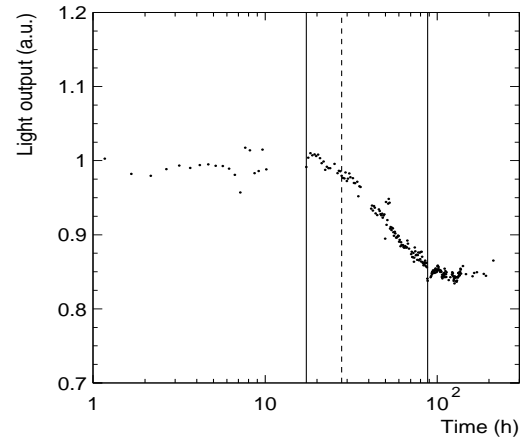

Figure 5: Relative attenuation of the light output from a Mitel VCSEL as a function of the time during a gamma irradiation. The vertical lines indicate the start and end of the irradiation period. Note the absence of annealing after the irradiation is completed. The dotted line denotes a 10 year LHC equivalent dose.

2.3 Multimode Fibre

Two 10 m long pieces of commercial off-the-shelf fibre have been irradiated with neutrons and gammas. The fi-

bres were not chosen for any particular reason, but rather to be representative of commercially graded index fibre. Due to the speed of the link, graded index fibre with a small core size is needed to ensure dispersion does not compromise the performance of the link. The first fibre is a piece of 50/125 germanium doped silica core 8-way fibre ribbon supplied by Acome. The second piece is a duplex patch cord supplied by Alcoa-Fujikura and designed for use with the transceiver modules described in section 2.1.

The fibres were arranged in coils to maximise the amount of fibre in the radiation beam. A 850 nm VC-SEL emitter was used to send light through the fibres and a calibrated optical multimeter used to measure the received amount of light. The emitter was monitored during the irradiation to check that the output power remained constant. Figure 6 (7) shows the induced attenuation during the neutron (gamma) irradiation. The induced attenuation in the
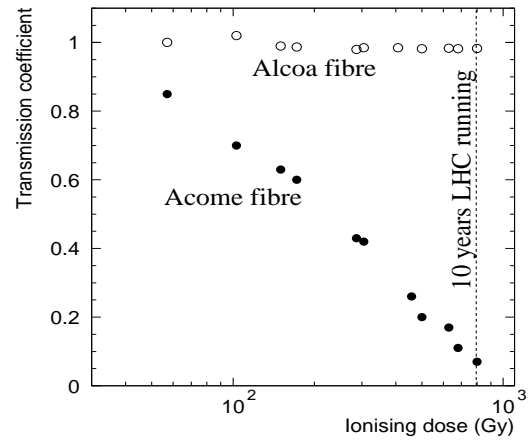

Figure 7: Gamma induced attenuation in 10 m lengths of two varieties of commercial graded-index fibre. The dotted line allows an extrapolation to the expected attenuation after 10 years of LHC running.

of frame lock which can result in a mean link-down time of 300 μs is needed. Results from the neutron and gamma irradiation of packaged VCSEL emitters and multimode fibre are also presented. Both brands of VCSEL are sufficiently radiation tolerant for use in LArg links. The radiation tolerance of the two off-the-shelf graded-index fibres tested differed greatly. One of the fibres would be suitable for use with LArg links. The reason for the marked difference in behaviour between the fibres is under investigation.

ACKNOWLEDGEMENTS

Figure 6: Neutron induced attenuation in 10 m lengths of two varieties of commercial graded-index fibre. The dotted line allows an extrapolation to the expected attenuation after 10 years of LHC running.

two fibres after a 10 year LHC equivalent dose is significantly different after both the neutron and gamma irradiations. The Alcoa-Fujikura fibre exhibits extremely good neutron and gamma radiation tolerance whereas the Acome fibre fails catastrophically during gamma irradiation.

3 SUMMARY

A serial optical link running at 1.6 Gb/s and based around the G-Link chipset and commercial VCSEL/PIN-diode transceiver units has been developed. The link fulfills the specifications of the readout links required for the AT-LAS LArg calorimeter and runs error-free in the laboratory for many days. Initial results on the neutron tolerance of the link are presented. The link satisfies total dose requirements if Methode transceivers are used, but further tests are needed to fully understand single event effects. In particular, a better understanding of errors induced by a loss

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Irradiation Test of the Single Event Upset Rate of the GLINK Transmitter/Receiver

Yong Li

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DUT: HDMP 1022 (TX), HDMP 1024 (RX)
Time: March 3, 2001, 7:00-9:30AM.
Location: Crocker Nuclear Laboratory, UC Davis
Proton beam energy: 63.3MeV
Active irradiation area: 2×2cm
Experimenters: Yong Li, Michael Medve, Carlos Castaneda (UCD)

Summary of Irradiation Test Result

Sample	Proton Fluence ($\times 10^{12}$/cm^2)†	# of Single-Bit-Errors	# of Link-Downs	Total Single-Event-Upsets	Total Ionizing Dose (Krad)†	Single Event Upset Error Rate (1 SEU per # protons/cm^2)	SEU rate at CSC worst location (1 SEU per # of hours)‡
RX 1	2.65	7368	2004	9372	356.72	2.827×10^8	8.14
RX 2	4.11	11116	2981	14097	553.25	2.915×10^8	8.39
RX 3	4.05	11051	2924	13975	545.34	2.898×10^8	8.34
RX 4	3.91	10179	2784	12963	526.41	3.016×10^8	8.68
TX 1	4.07	11721	1444	13165	548.00	3.091×10^8	8.90

†*The statistical error for the total proton fluence and the total ionizing dose is ≈1.6%.*
‡*The statistical error for the SEU rate at the location of worst radiation of CSC is less than 2%.*

The DAQ was started before the proton beam stop was lifted and we saw no error without irradiation. After the beam stop was lifted and protons were dumped at the DUT, SEU errors were seen immediately. After the scheduled beam time was reached, beam stop was placed back into the proton beam to block further irradiation, the GLINK tester was still running perfectly and no more errors were logged. This phenomenon proved that the errors logged were indeed induced by proton irradiation and the system was robust.

Some arguments:

- The standard we set for qualifying the GLINK components is one SEU error per 42 minutes, assuming each upset causes link-down and the tolerable data loss is less than 0.1% for the whole CSC system. The tested result is about 70 times better than the standard.
- The fluence of neutrons with E>20MeV at the location of worst radiation of CSC in 10 years is 1.5×10^{12} /cm^2.
- This result definitely qualifies the HDMP 1024 (receiver). The HDMP 1022 (transmitter) should also be qualified, since it is manufactured with the same technology. Unfortunately I didn't have enough good TX samples.

The distributions of link-down time in μs:
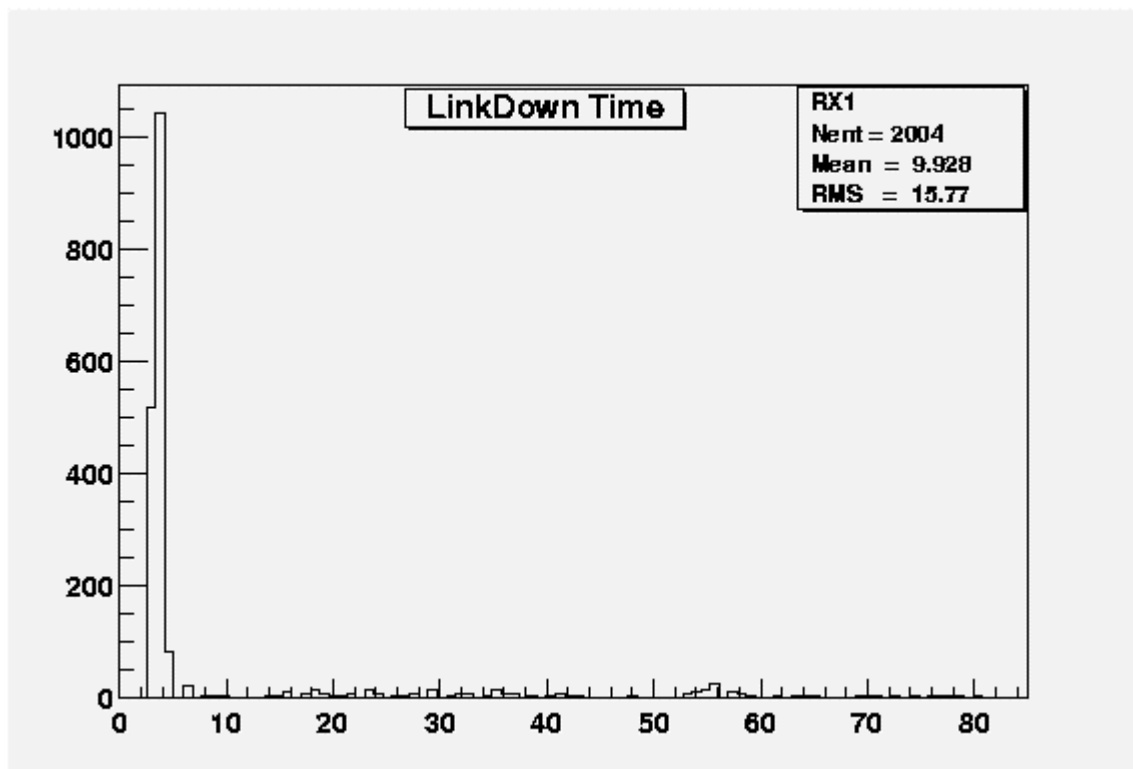
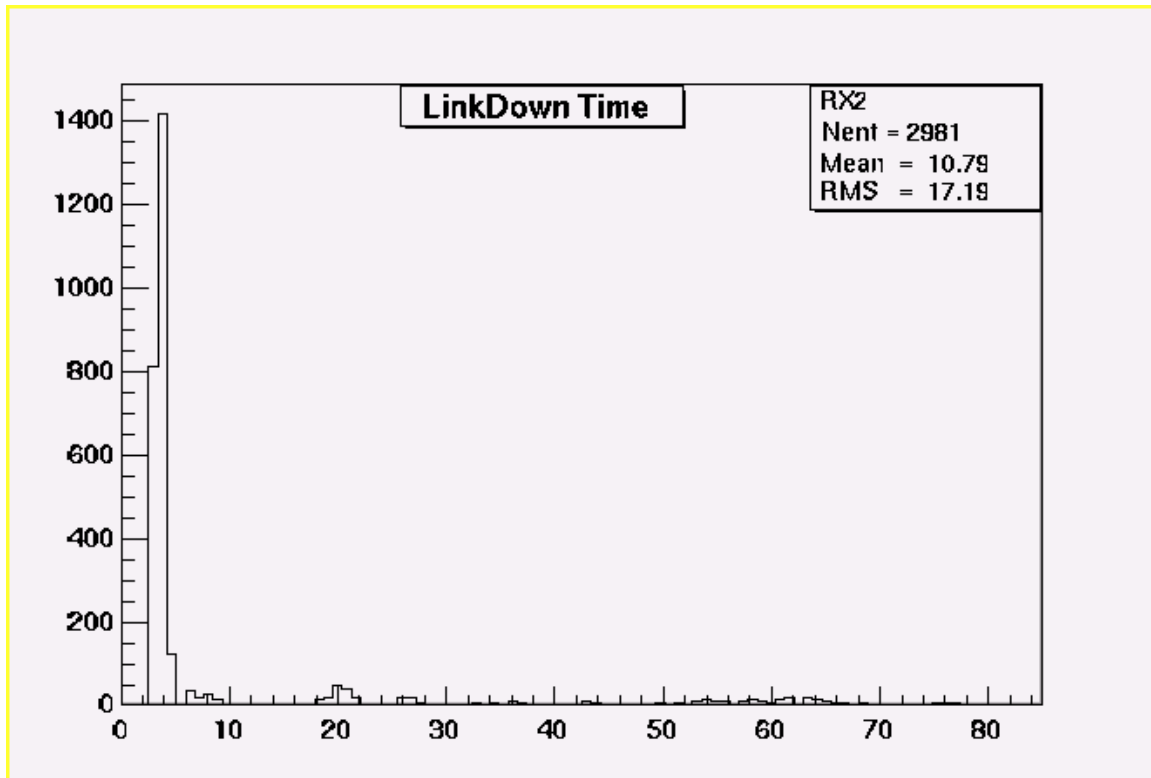Figure 1. The link-down time distribution of RX1

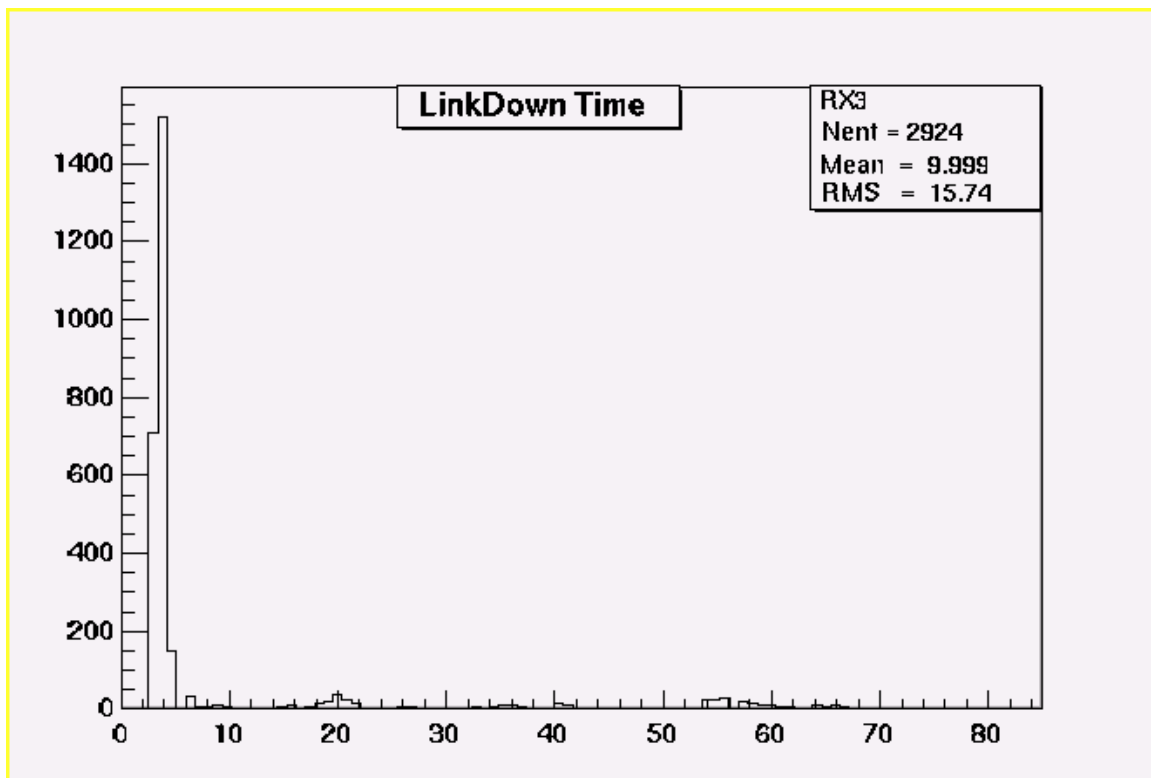Figure 2. The link-down time distribution of RX2.

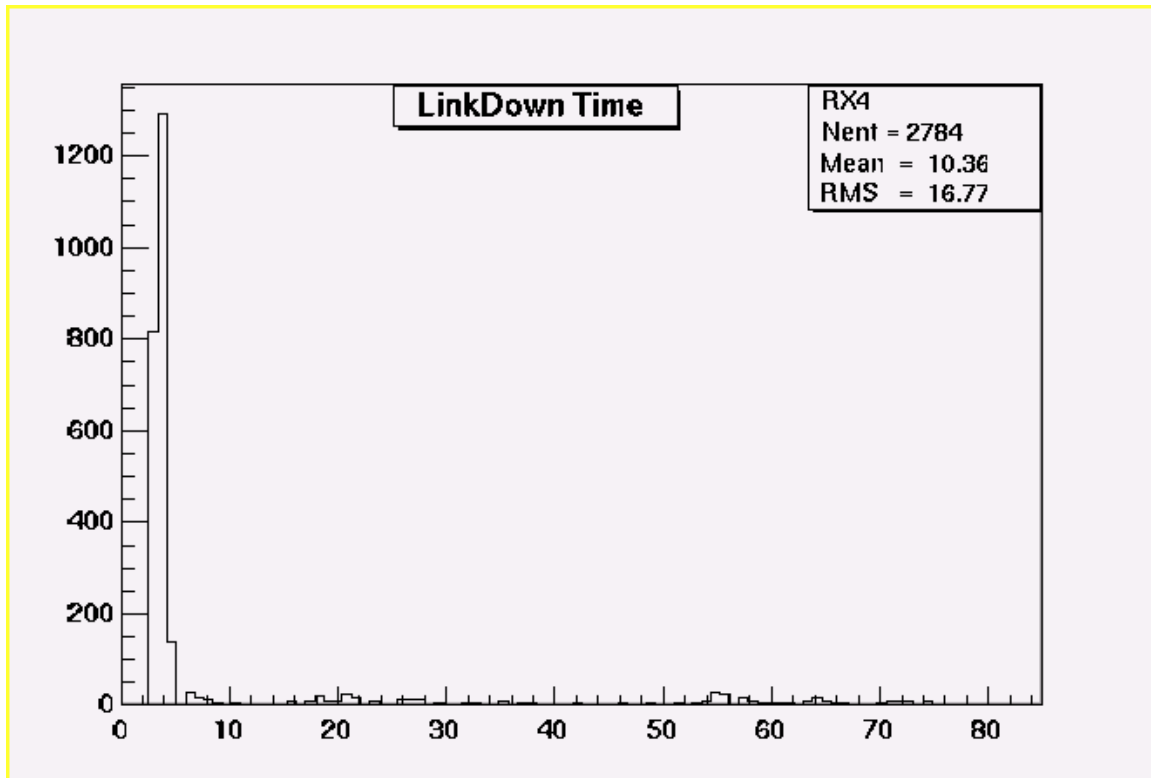
Figure 3. The link-down time distribution of RX3.
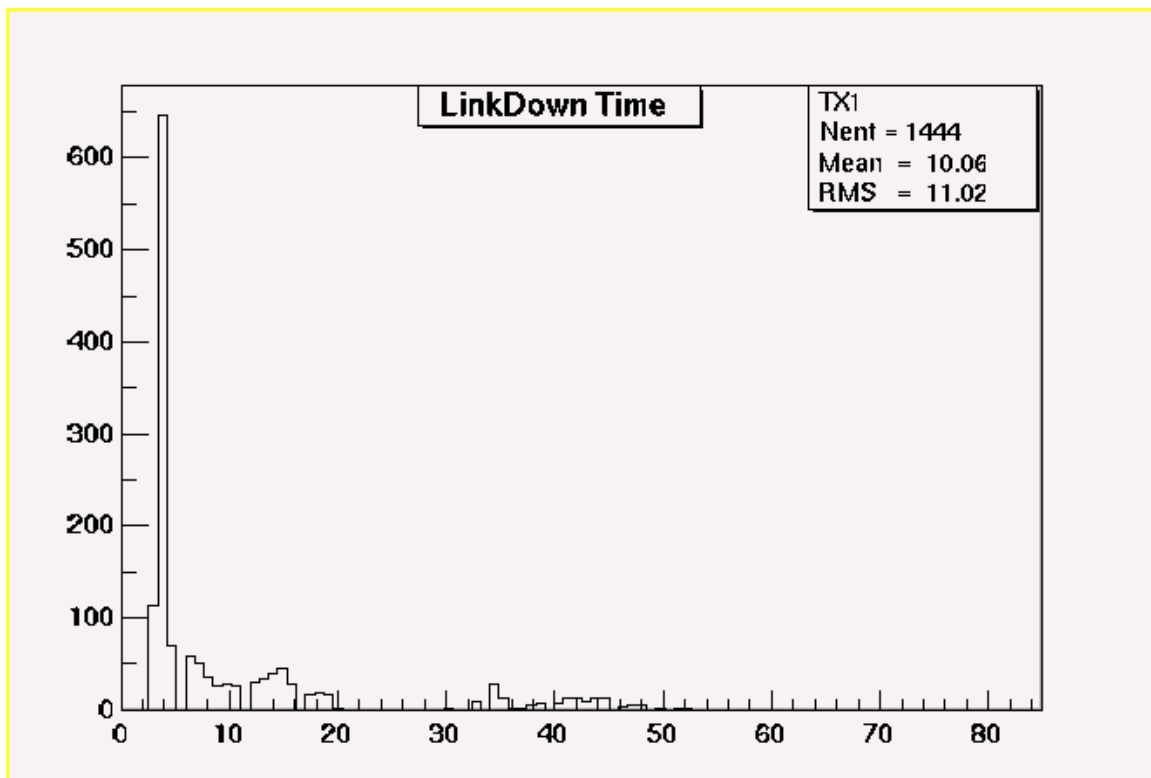
Figure 4. The link-down time distribution of RX4.

Figure 5. The link-down time distribution of TX1.